An 11-bit 45MS/s pipelined ADC with rapid calibration of DAC errors in a multi-bit pipeline stage

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Overview

• Motivations
• State of the art
• Approach of this work
  – Rapid calibration of gain and DAC errors in 1st pipeline stage
  – Design in 0.18µm CMOS
• Measurement results
• Summary
Motivations: ADC non-idealities

• **Background digital** calibration effects of:
  1.) Capacitor mismatch
  2.) Small DC opamp gain
Why Short calibration time?

- Long calibration time limits testing throughput
- \(2^{2N}\) cycles for gain calibration with statistical techniques (empirical)

[Ray, Song, JSSC March ’07] \(10^7\) cycles for 80dB SFDR
[Siragusa, Galton, JSSC Dec ’04] \(10^8\) cycles for 90dB SFDR

- E.g. \(10^7\) clock cycles for calibration, 45MS/s
  \(\rightarrow\) 220ms to test calibration
State of the art: Split ADC

- [Li, Moon, TCAS-II, Sept 2003], [McNeill et al, ISSCC 2005]
  - Corrects opamp gain error in very short time
- We expand concept in this work to also correct for DAC errors
4-bit pipeline stage residue: ideal

MSB  0  1  2  3  •  •  •  13  14  15

$V_{\text{ref}}$

output

$-V_{\text{ref}}$

$-V_{\text{ref}}$  input  $V_{\text{ref}}$

$V_{\text{ref}}$
4b Residue with Gain errors

MSB 0 1 2 3 \cdots 13 14 15

V_{\text{ref}}

output

-V_{\text{ref}}

-V_{\text{ref}} \quad \text{input} \quad V_{\text{ref}}

8(1-\gamma)
With Gain and DAC errors

- Gain errors special case of DAC errors $\rightarrow \delta(i) = \delta$
- Thus Correcting DAC errors, also corrects gain errors
1\textsuperscript{st} stage residues in this work

**Stage 1 residue, ADC A**

MSB\textsubscript{A}:

| 0 | 1 | 2 | 15 |

**Stage 1 residue, ADC B**

MSB\textsubscript{B}:

| 0 | 1 | 2 | 15 | 16 |

ADC A

3+1b stage

Backend ADC

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ADC B

3+1b stage

Backend ADC
1st stage residues: no errors

Output of ADC A

Output of ADC B

\[ \text{MSB}_A \quad \text{LSB}_A \quad \text{MSB}_B \quad \text{LSB}_B \]

Output of ADC B

\[ \Delta_{(i+1)2} \quad \Delta_{i1} \quad \Delta_{i2} \quad \Delta_{(i+1)1} \]
1st stage residues: with DAC errors

- ADC A used as ideal reference to measure errors of ADC B
- single DAC error measured with minimum of 2 clock cycles

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ADC A: error measurement

- Calibration requires input to be sufficiently busy to excite each MSB
Digital Error IIR filter

- Use average error to minimize noise and input dependency
- \( \mu \) a power of 2 for simple implementation

\[ \Delta_i \rightarrow \mu \rightarrow + \rightarrow \mu^{-1} \rightarrow z^{-1} \rightarrow \Delta_i \]
Digital correction of errors
Calibration architecture in full

- Include LMS adaptive term $\alpha$ to match ADC gains
• Gain reduced from 8x to 4x → larger feedback factor
5-bit Flash ADC - comparator

- Array of comparators used for 5-bit flash
- Resistor string used for Flash ADC reference voltages
- Preamp to reduce offset, minimize kickback
Testability: Process variation
0.18µm CMOS Chip Micrograph

- Area = 3.57mm$^2$
- Power = 81mW (analog core)
INL improved from +6.4/-6.1 to +1.1/-1.0 LSB
Before calibration
SFDR=48.9dB
SNDR=46.9dB

After calibration
SFDR=70dB
SNDR=60dB
Accuracy improvement over time

- 11-bit linearity within $10^4$ cycles (i.e. 0.22ms)
- Compare to $2^{2(11)} = 4 \times 10^6$
- Verified with different ‘busy’ full scale inputs
Performance summary

\[ f_s = 45 \text{MS/s} \ (f_{\text{in}} = 2.39 \text{MHz}) \]

<table>
<thead>
<tr>
<th></th>
<th>Before calibration</th>
<th>After Calibration</th>
</tr>
</thead>
<tbody>
<tr>
<td>INL (LSB)</td>
<td>+6.4/-6.1</td>
<td>+1.1/-1.0</td>
</tr>
<tr>
<td>SFDR (dB)</td>
<td>48.9</td>
<td>70</td>
</tr>
<tr>
<td>SNDR</td>
<td>46.9</td>
<td>60</td>
</tr>
<tr>
<td>Power (analog core)</td>
<td>81mW</td>
<td></td>
</tr>
<tr>
<td>Area</td>
<td>3.57mm²</td>
<td></td>
</tr>
<tr>
<td># calibration cycles</td>
<td>10^4 cycles, (0.22ms)</td>
<td></td>
</tr>
</tbody>
</table>
Conclusions

• Presented architecture to rapidly correct DAC and gain errors in multi-bit pipeline stage

• Measured results in 0.18µm CMOS show linearity improved by >3b within $10^4$ clock cycles

• Calibration achieved in more than two order of magnitude fewer clock cycles than prior statistical approaches
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