An 11-bit 45MS/s pipelined ADC with rapid calibration of DAC errors in a multi-bit pipeline stage

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Abstract—**A technique to rapidly correct for DAC errors in the multi-bit first stage of an 11-bit pipelined ADC is presented. Using a split-ADC approach the digital background scheme is validated with a proof-of-concept prototype fabricated in 1.8V 0.18µm CMOS, where the calibration scheme improves the INL of the ADC at f_s=45MS/s, from +6.1/-6.4LSB to +1.1/-1LSB after calibration. The SNDR/SFDR is improved from 46.9dB/48.9dB to 60.1dB/70dB after calibration. Calibration is achieved in ~10^4 clock cycles.**

I. Introduction

Capacitor mismatch is a major source of missing codes that degrade accuracy and linearity in the output of pipelined ADCs. Large capacitor areas can be used to improve matching, however at the penalty of increased power consumption to maintain a fixed settling accuracy. Additional layers can also be used to implement well matched MiM capacitors, although extra layers can increase fabrication costs and matching typically is limited to ~0.1%.

With migration to deeper submicron technologies and lower supply voltages, it has become increasingly attractive to implement techniques which can measure and correct ADC non-idealities in the digital domain. Several background and foreground techniques to digitally calibrate DAC errors in pipelined ADC stages have been proposed in recent years (e.g. [1], [2], [3]). Background techniques have the advantage of continuously measuring and correcting ADC non-idealities without interrupting normal operation. Foreground calibration techniques however can derive correction parameters with significantly fewer clock cycles than background approaches.

Previously published background approaches primarily use statistical techniques to estimate correction parameters (e.g. [1], [2]), where a large number of ADC outputs (hence long calibration time) are required to derive an accurate estimate of the correction terms. E.g. in [2] $8x10^7$ cycles are required to achieve 13-b linearity. For gain only calibration statistical techniques typically take 2^{2n} clock cycles (where n is the resolution in bits) [4]. A short calibration time is highly desirable in industry as long calibration times limit the number of ICs which can be tested before deployment in a mass production environment during a fixed time interval.

In this work a split-ADC approach is used to attain calibration in a short time interval. Previous split-ADC techniques [5], [4] have discussed methods to correct for gain errors in 1.5b/stages. In this work we show how the concept can be extended to also rapidly correct for DAC errors in multi-bit pipeline stages using a simple digital realization. A proof-of-concept 11-bit pipelined ADC prototype was fabricated in a 1.8V 0.18µm CMOS process, where the calibration scheme was used to correct DAC errors in the 4-bit first stage of each split-ADC. Measured results show an improvement of the ADCs INL from +6.1/-6.4LSB to +1.1/-1LSB after calibration. The SNDR/SFDR is improved from 46.9dB/48.9dB to 60.1dB/70dB after calibration. Calibration is achieved in ~10^4 clock cycles.

II. DAC Error Calibration Architecture

A. Review of error sources

Fig. 1 illustrates a 4-bit pipeline stage with 1-bit overlap to allow for sub-ADC errors, and Fig. 2 illustrates the ideal residue transfer function of the stage output.

Finite DC opamp gain represented by an error term γ reduces the slope of each linear segment in Fig. 2, resulting in a constant number of missing codes where MSB bits change (i.e. constant DNL errors or constant jumps in INL). Prior split-ADC algorithms and the majority of prior calibration schemes are concerned with estimating γ and digitally compensating for it by scaling the backend code by $(1-\gamma)^{-1}$.

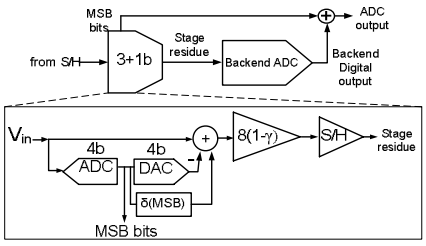

Fig. 1: 3-bit first stage with extra bit of redundancy

DAC errors however are a function of the MSB bits resolved and cause each linear segment of the residue in Fig. 2 to be shifted up or down by different static random values δ(i) as shown in Fig. 3, thereby introducing non-constant missing codes at every MSB transition. As the missing codes are non-constant a gain calibration scheme cannot be used to digitally correct the ADC output. A separate adaptive term for *each* MSB transition is required for calibration, significantly increasing the complexity of the correction scheme over gain-

only correction techniques. For a 4-bit pipeline stage with 1-bit of redundancy 15 correction parameters for 16 unique DAC outputs are required to be estimated.

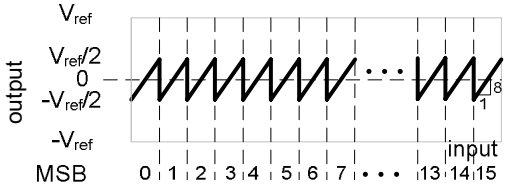

Fig. 2: ideal residue transfer function of first stage

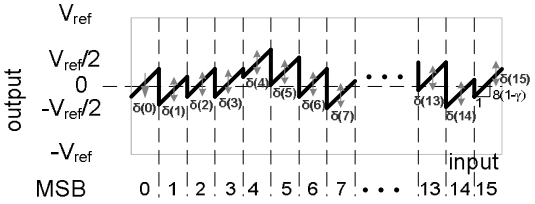

Fig. 3: residue transfer function w/gain and DAC errors

Missing codes produced by gain errors are a special case of missing codes produced by DAC errors where the number of missing codes at each MSB transition is constant. Thus a calibration scheme which corrects for the missing codes as a function of each MSB, also corrects both DAC and gain errors. DAC calibration schemes require all MSB bits to be exercised to measure each unique DAC error. Since MSB bits can change only once every clock cycle DAC calibration schemes can require N-1 times more cycles to converge (where N is the number of unique MSB outputs) than gain calibration schemes where the correction parameter estimated is not a function of the MSB. Thus it is even more critical in DAC error correction schemes that calibration time be small.

B. Calibration scheme

In the calibration scheme of this work two ADCs (ADC A and ADC B) simultaneously process in parallel the same analog input as shown in Fig. 4. The final ADC output is generated by the average of the two ADC outputs, thus each ADC is designed with half the total capacitance, hence half the power and area of the overall ADC to meet thermal noise requirements [5]. From Fig. 4 ADC A and B are identical except in each ADC the residue transfer function in the first stage is horizontally offset from the other by ½ MSB.

From Fig. 5 if the analog input to the ADC is such that MSB_A=i, then MSB_B is either i or i+1. The offset between the digital outputs of ADCs A and B for the range of analog inputs where MSB_A=i and MSB_B=i is denoted Δ_{i1}, and Δ_{i2} where MSB_A=i and MSB_B=i+1 as shown in Fig. 5. In an ideal ADC $\Delta_{i1}=\Delta_{i2}$ (Fig. 5) however with DAC and/or gain errors the difference between Δ_{i1} and Δ_{i2} is precisely the error due to missing codes that occurs when MSB_B changes from i to i+1 as shown in Fig. 6. An accurate measure of Δ_{i1} and Δ_{i2} (thus accurate measure of error) can be made by simply measuring the average values of Δ_{i1}, Δ_{i2}, using a first order IIR filter with transfer function $\mu/[1-(1-\mu)z^{-1}]$ as shown in Fig. 7. In other words, the output of ADC A is used as an ideal reference for ADC B when MSB_A=i to measure $\bar{\Delta}_{iB}=\bar{\Delta}_{i1}-\bar{\Delta}_{i2}$. In a similar manner the error due to missing codes at all other MSB transitions can be measured for ADC B. Errors due to missing codes for ADC A are measured by noting that $\Delta_{i2}-\Delta_{(i+1)1}$ is the error due to missing codes in ADC A when MSB_A changes from i to i+1 as shown in Fig. 6. Hence the missing code errors in ADC A can be determined using already measured values $\bar{\Delta}_{i2}-\bar{\Delta}_{(i+1)1}$. Errors due to missing codes at all other MSB transitions in ADC A are measured using an identical extension as done for ADC B.

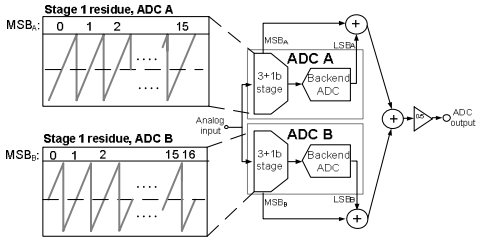

Fig. 4: Split ADCs with different 1st stage

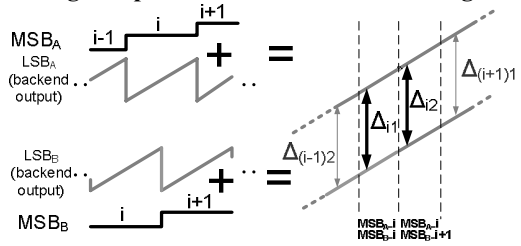

Fig. 5: offset between ADCs A, B w/no gain, DAC errors

With the errors from missing codes at each MSB transition measured, each ADC is corrected by shifting each ADC's digital output as a function of MSB such that overall transfer function of each ADC is free from missing codes due to errors in the first stage as shown in Fig. 8 (same done for ADC A).

Rapid background calibration is achieved as every analog input while MSB_A=i produces outputs in ADCs A and B which when subtracted immediately give estimates of Δ_{i1} or Δ_{i2}. In contrast statistical techniques use statistical correlations which require many output samples to extract similar information. As long as the input is sufficiently busy to generate a sufficient number of estimates of Δ_{i1}, Δ_{i2}, for all i, there is no constraint on the type of input signal to the ADC.

It is noted that the approach of this work is very similar to background calibration techniques where more accurate but slower ADCs operate in parallel to the ADC under calibration [3]. In this work however, since the residue transfer function of one of the split ADCs is offset, ADC A does not suffer an error in the first stage for the same input as ADC B, thus one ADC can be used as an ideal reference for the other, eliminating the need for one of the ADCs to be more accurate than the other. Hence there is no need to trade higher accuracy with lower sampling rates in the second ADC; both ADCs can operate at the same speed, and both ADCs be used to digitize the analog input. Thus the power of the additional ADC also goes towards lowering the noise floor in the digital output, unlike [3] where the additional ADC (since it operates slower) only aids the correction scheme. Furthermore using the

technique outlined in this work both ADCs are calibrated whereas in [3] only one ADC is.

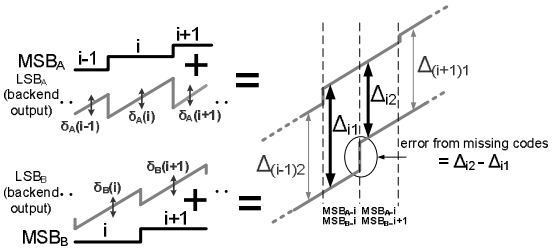

Fig. 6: Offset between ADC A, B w/ gain, DAC errors

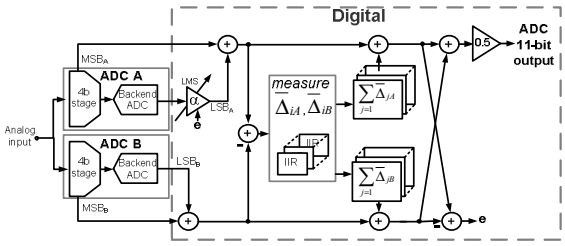

Fig. 7: Digital correction of DAC and gain errors

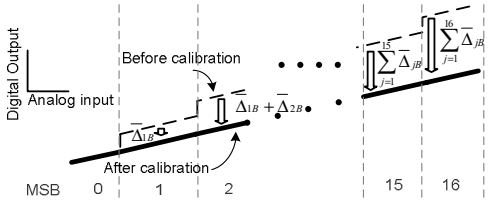

Fig. 8: Correction of DAC, gain errors in ADC B w/$\bar{\Delta}_{iB}$

C. Gain mismatch

Due to random mismatches, the first stage of ADC A in Fig. 1 will have a slightly different gain and offset when compared to ADC B. A constant offset between ADC A and B is common-mode as it is eliminated by subtracting $\bar{\Delta}_{i2}$ from $\bar{\Delta}_{i1}$. To account for gain mismatch between the two ADCs an LMS adaptive gain term (α in Fig. 7) is also included which scales the backend code of ADC A so as to keep the outputs of ADC A and B parallel.

Ultimately, the accuracy of estimation in errors due to missing codes in the first stage is limited by missing codes and distortion in the backend, which although not addressed in this work can be minimized by also calibrating the backend stages.

III. Circuit Implementation

Fig. 9 shows the architecture of the 11-bit pipeline ADC of this work. An additional three bits are added to the backend in each split-ADC to improve the accuracy in error estimation.

To ensure both ADCs operate on the same analog input, a conventional flip-around front-end sample-and-hold was used. Thermal noise of the entire ADC was 11-bit input referred.

The MSB transitions for each split ADC were generated by a single 5-bit flash ADC where even outputs were used for ADC A and odd outputs for ADC B. Fig. 10 shows the comparators used in the 5-bit flash. Reference voltages for the flash ADC were generated using a resistor string. A preamp is used in each comparator to minimize kick back onto the reference voltage resistor string.

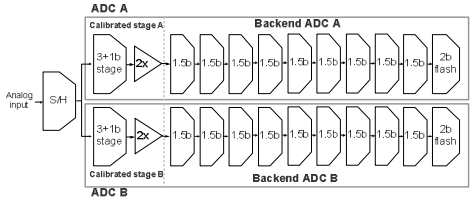

Fig. 9: Pipelined stages in each ADC

The architecture of the multi-bit MDAC in the first stage of ADC A is shown in Fig. 11. The first stage in ADC B is similar but slightly modified for a ½MSB horizontal offset. To enable testability for a spread of capacitor mismatches without testing thousands of chips for random variation, each sampling capacitor in the first stage of each split ADC was made individually digitally programmable with 0.5%, 1% and 5% deviations from nominal values. For ease of implementation in this prototype the calibration scheme requires the input to be sufficiently busy to excite each sampling capacitor to achieve full calibration. However it is possible to relax the input signal swing requirement by rotating the sampling capacitors in a sequence not correlated with the analog input. A folded cascode opamp with DC gain of only 50 dB was used in Fig. 11 as the gain error in the first stage was corrected.

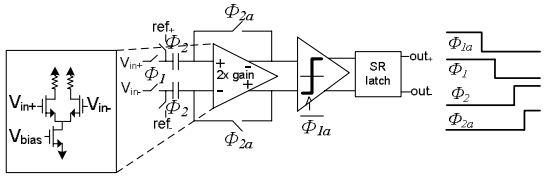

Fig. 10: Comparator architecture

Since a large closed loop DC gain requires a large open loop unity gain frequency for high sampling rates, and is very sensitive to opamp input capacitance (which can be on the order of the sampling capacitance) the closed loop gain of the first pipeline stage in each ADC was reduced from 8x to 4x. To compensate for the gain reduction, the first stage was followed by a pipelined stage which only implemented a 2x gain. The trade off in distributing the gain of the first stage over more than one stage is an increase in ADC latency.

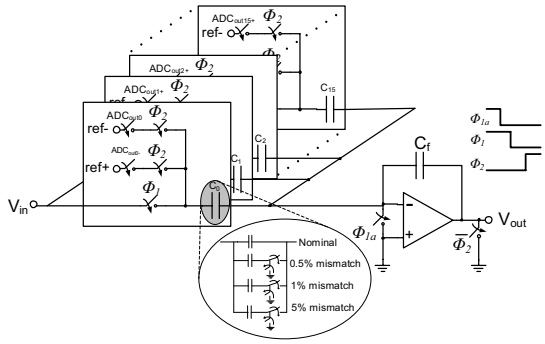

Fig. 11: 1st stage MDAC for ADC A

The backend ADC was implemented with standard 1.5b/stage pipeline stages. Gain-boosted folded cascode opamps with a DC gain of 95dB were used in stages 2 and 3 to minimize missing codes in the backend. Remaining stages used folded cascode opamps with DC gains of 50dB.

IV. Measured Results

A prototype of the ADC architecture as shown in Fig. 12 with a core area of 3.57mm^2 was fabricated in a 1.8V 0.18µm CMOS process. The ADC was operated at f_s=45MS/s where the power of the ADC was 81mW plus 9.5mW for all reference voltage resistor strings. To enhance flexibility in testing of the prototype, the digital outputs of each split ADC stage were taken off chip and imported into Matlab via a logic analyzer, where the digital outputs of the fabricated chip were input to a model of the calibration scheme outlined in this work. Since there is no feedback or direct interaction with the analog portions of the ADCs in the calibration scheme of this work, operating on the off-chip digital outputs verifies the calibration scheme without any loss of generality.

Fig. 13 shows the INL of the ADC before and after calibration with each DAC element in each split ADC programmed with different mismatches. The INL is improved from +6.1/-6.4LSB to +1.1/-1LSB after calibration, and DNL from +1.1/-0.4LSB to +0.45/-0.4LSB. From Fig. 13, INL errors due to missing codes in the first stage are minimized; the remaining INL errors are dominated by distortion in the backend ADCs and front-end sample and hold. Fig. 14 shows an FFT of the ADC output before and after calibration with a 1.3V p-p sinusoid at 2.39MHz. The SNDR/SFDR of the ADC is improved from 46.9dB/48.9dB to 60.1dB/70dB. The calibration technique was verified with different programmed mismatches in the first stage as well as different full scale inputs (e.g. sinusoidal, random). In all cases successful background calibration was attained in ~1x10^4 clock cycles or effectively 0.22ms (with µ=1/64). Fig. 15 shows convergence of ADC accuracy with calibration time.

V. Conclusions

A technique to rapidly measure and correct for missing codes introduced by a multi-bit first stage in a pipelined ADC was presented. Measured results from a prototype in 1.8V 0.18µm CMOS show INL can be improved from +6.1/-6.4LSB to +1.1/-1LSB, and SNDR/SFDR from 46.9dB/48.9dB to 60.1dB/70dB using the approach of this work. Calibration is achieved in ~10^4 clock cycles.

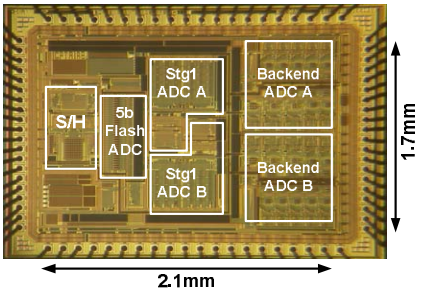

Fig. 12: Micrograph of prototype in 1.8V, 0.18µm CMOS

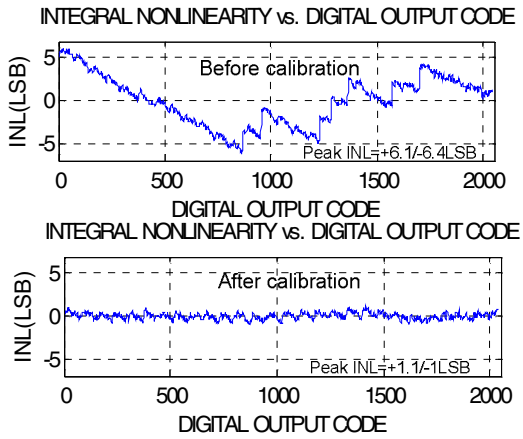

Fig. 13: INL before and after calibration

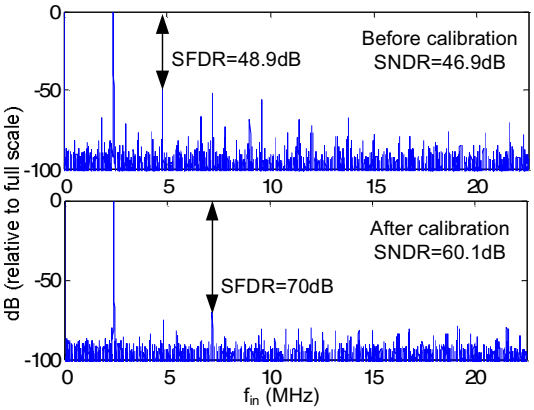

Fig. 14: Output FFT before/after calibration, f_{in}=2.39MHz

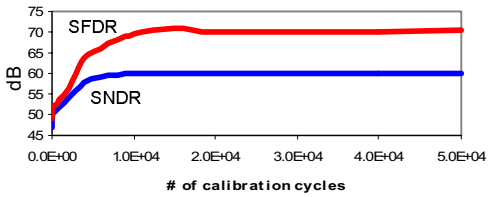

Fig. 15: SNDR/SFDR improvement with calibration cycles

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