ESSCIRC 2007
Session A3L-G1

An 11-bit 45MS/s pipelined ADC with rapid calibration of DAC errors in a multi-bit pipeline stage

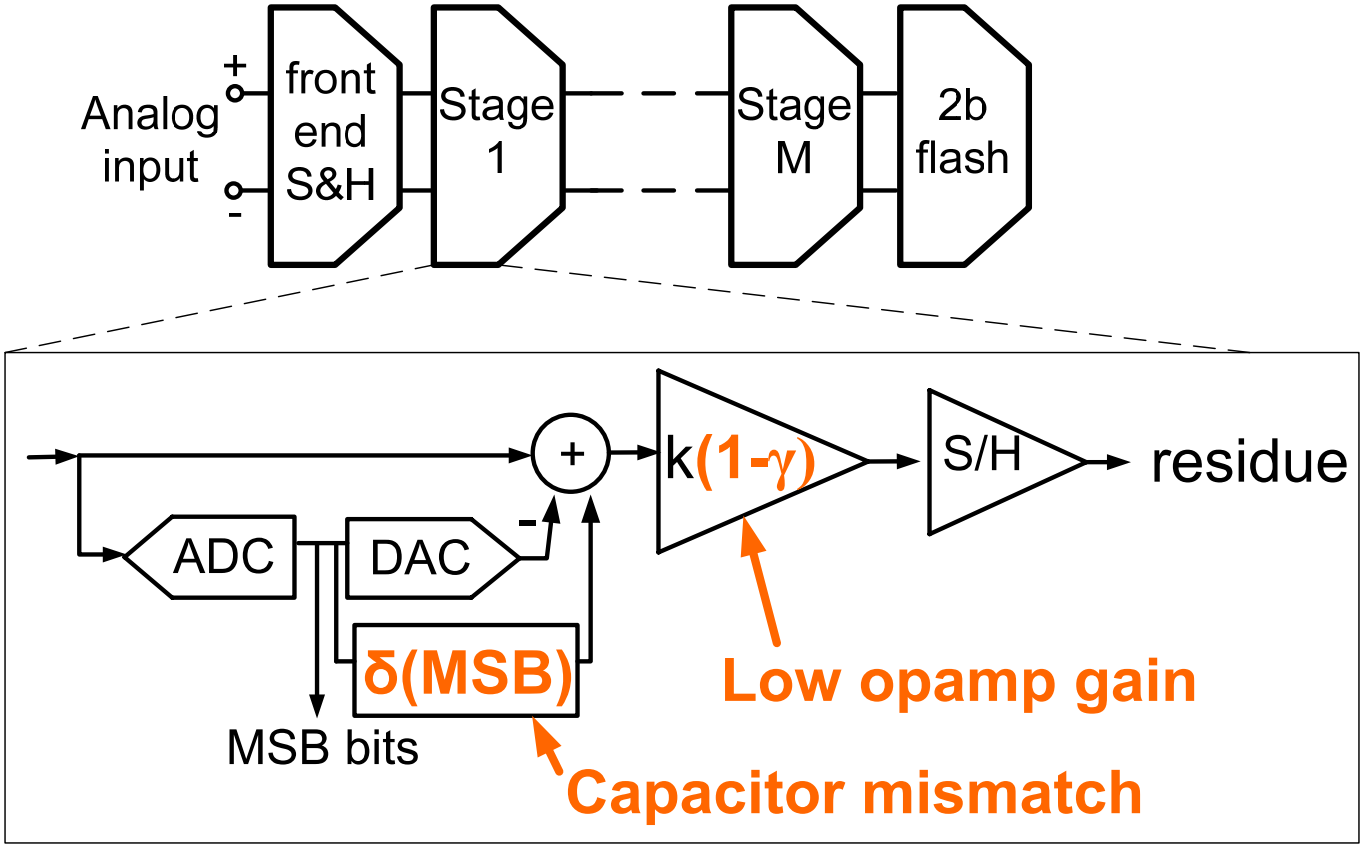
Imran Ahmed, David A. Johns
University of Toronto

University of Toronto
Department of Electrical and Computer Engineering

Overview

- Motivations
- State of the art
- Approach of this work
  - Rapid calibration of gain and DAC errors in 1st pipeline stage
  - Design in 0.18μm CMOS
- Measurement results
- Summary

Motivations: ADC non-idealities



- **Background digital** calibration effects of:
  - **1.)** Capacitor mismatch
  - **2.)** small DC opamp gain

Why Short calibration time?

- Long calibration time limits testing throughput
- **2^{2N}** cycles for gain calibration w/statistical techniques (empirical)

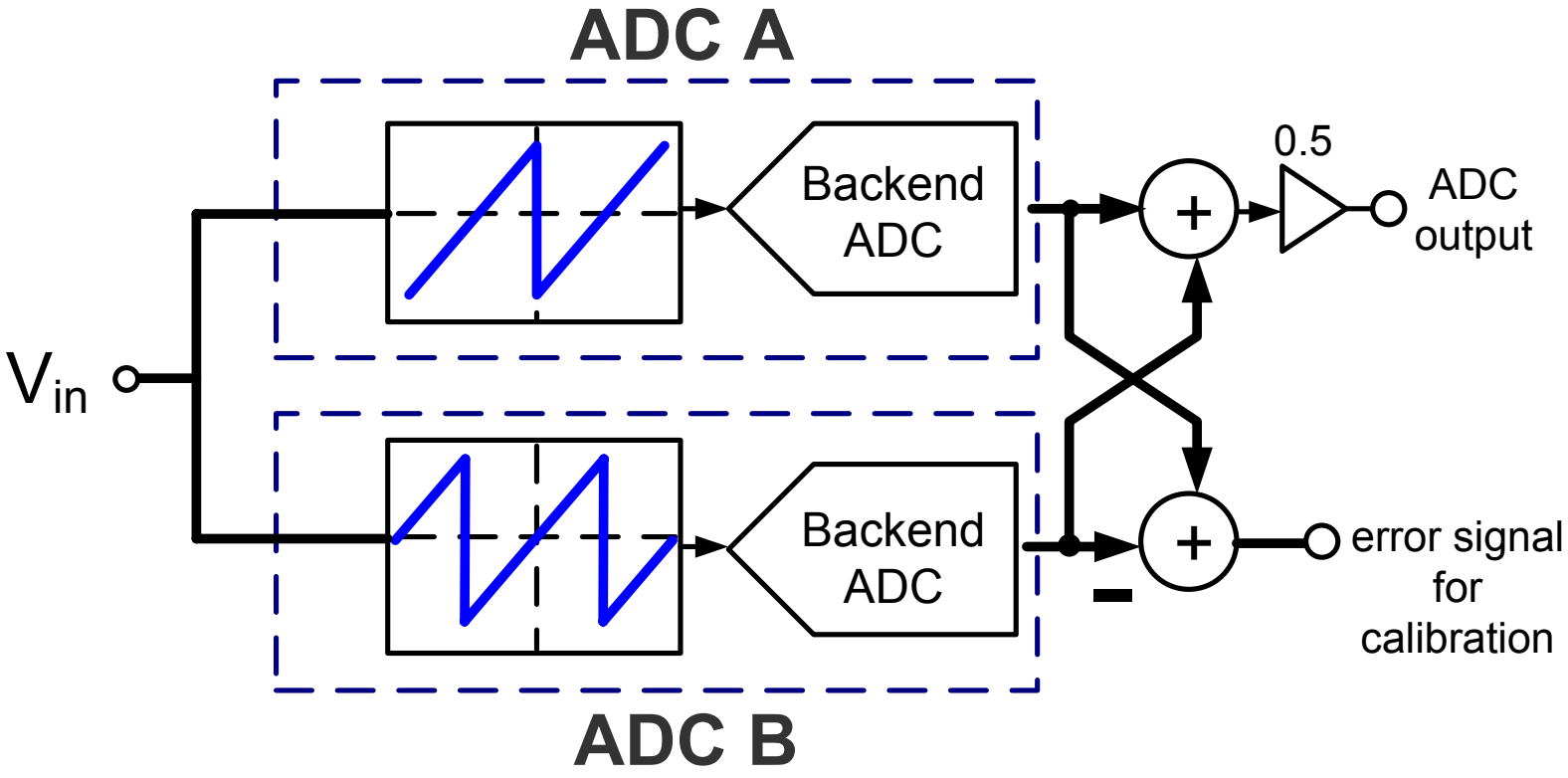
[*Ray, Song, JSSC March '07*] **10^7** cycles for 80dB SFDR

[*Siragusa, Galton, JSSC Dec '04*] **10^8** cycles for 90dB SFDR

  - E.g. 10^7 clock cycles for calibration, 45MS/s

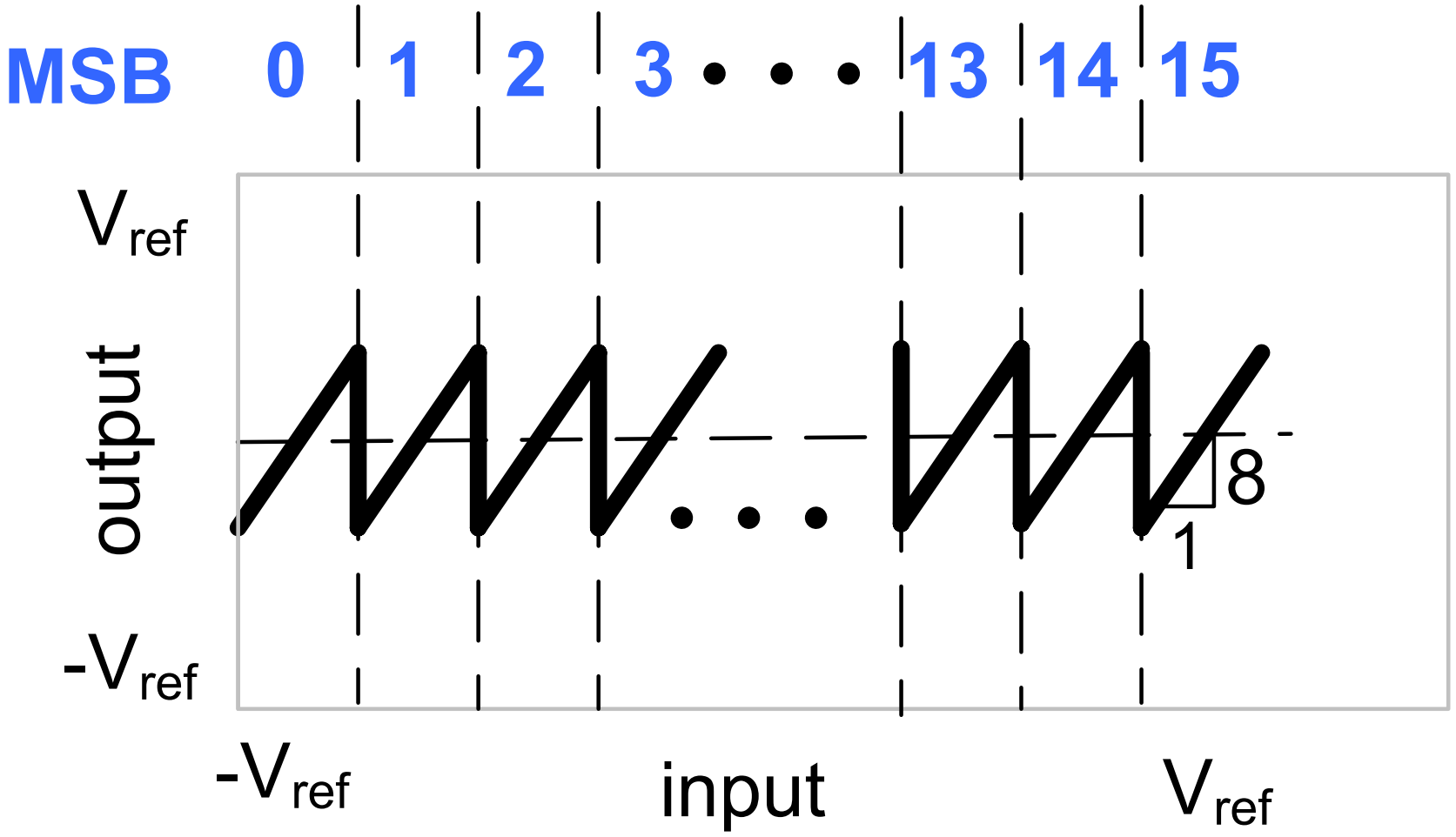
    → 220ms to test calibration

State of the art: Split ADC

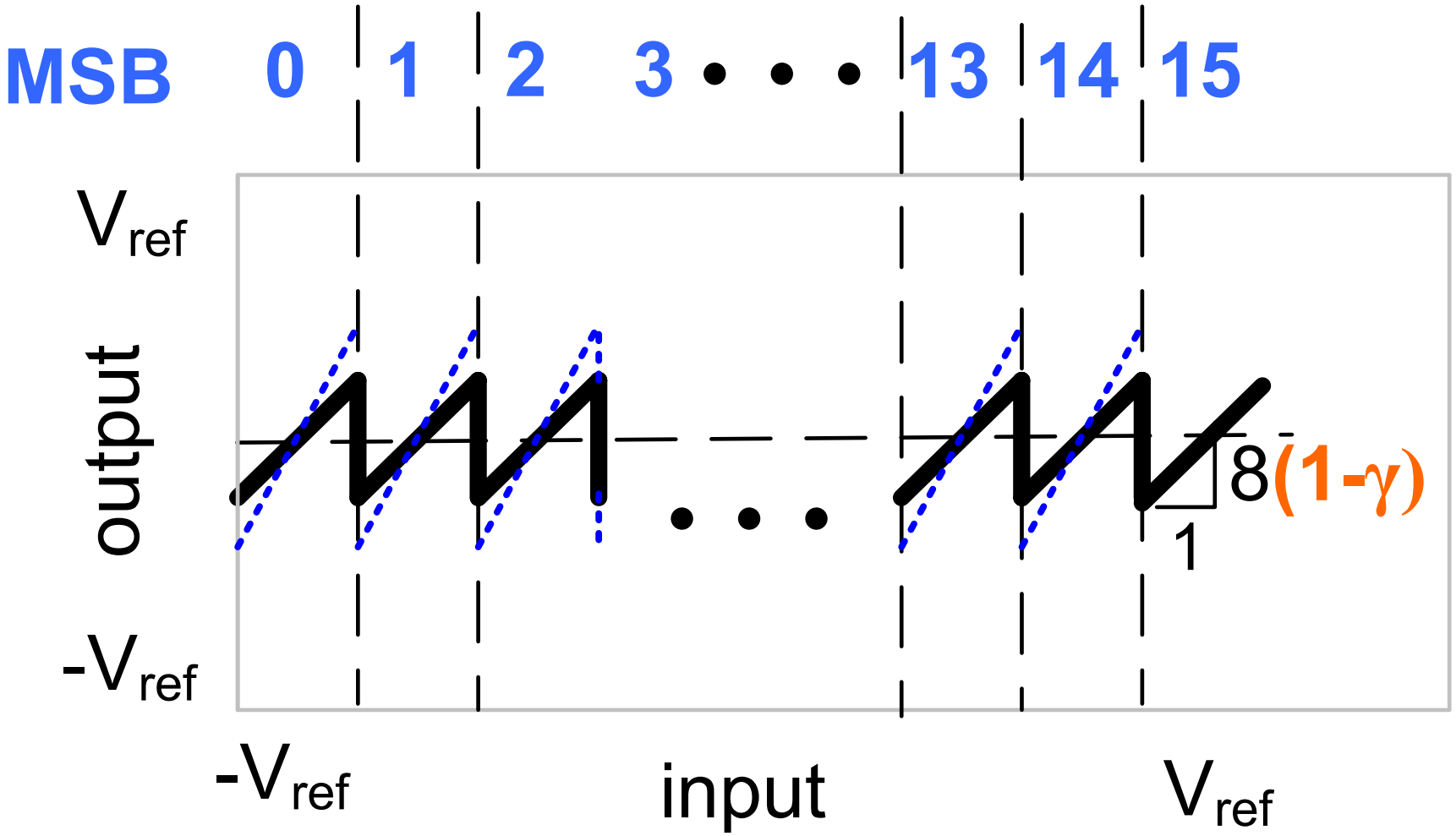


- [Li, Moon, TCAS-II, Sept 2003], [McNeill et al, ISSCC 2005]
  - Corrects opamp gain error in very short time
- We expand concept in this work to **also** correct for DAC errors

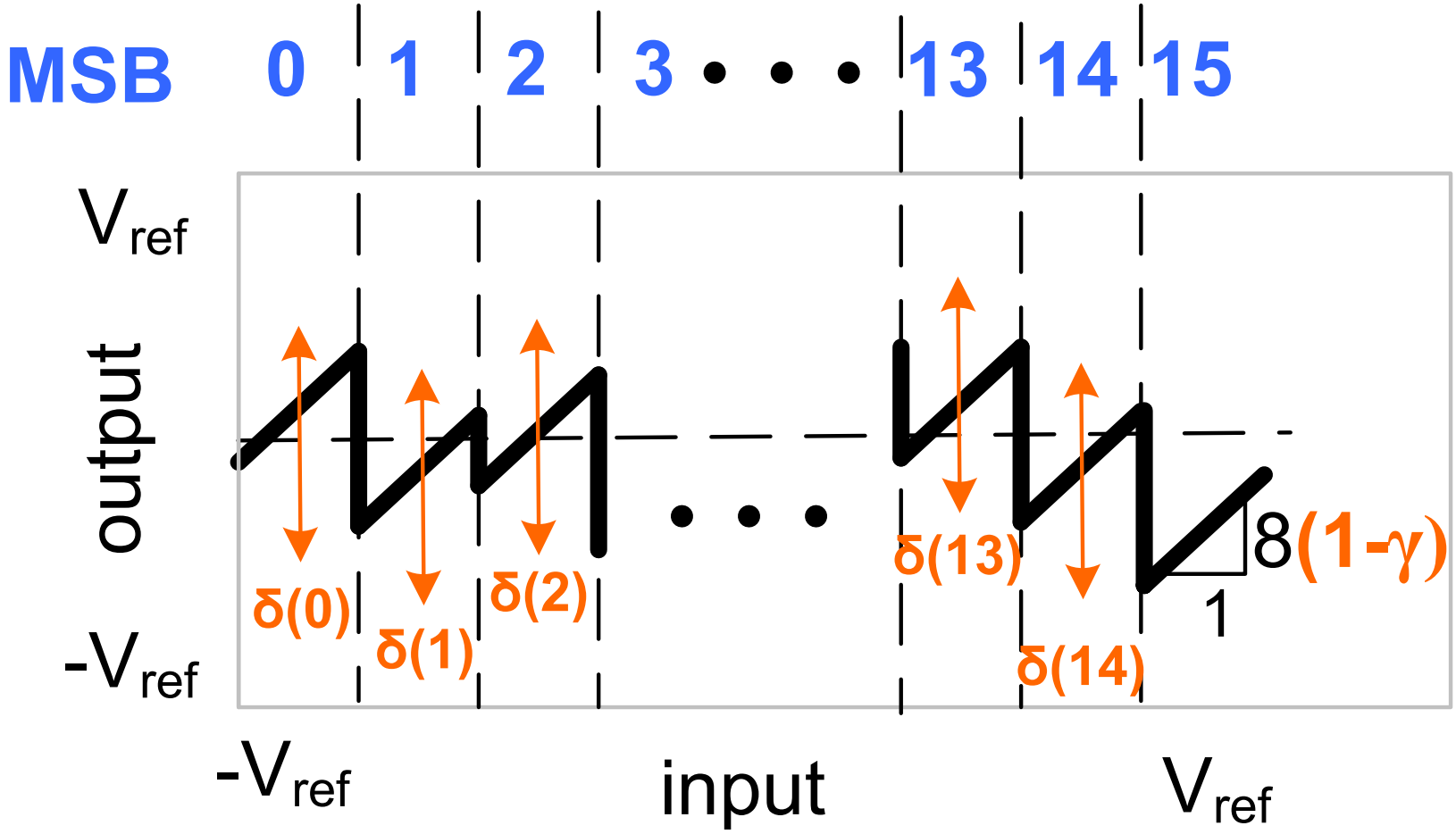
4-bit pipeline stage residue: ideal



4b Residue with Gain errors

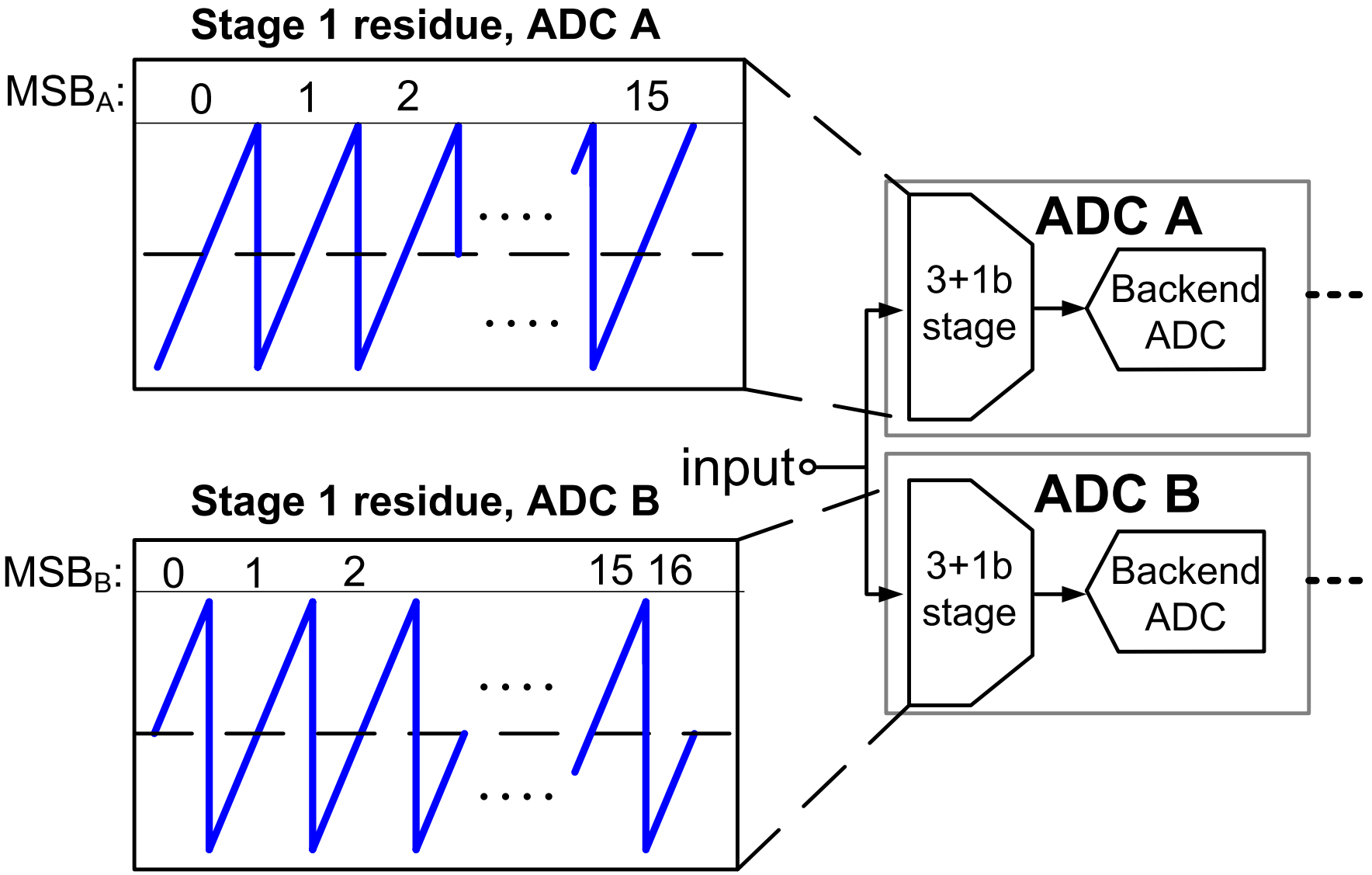


With Gain and DAC errors

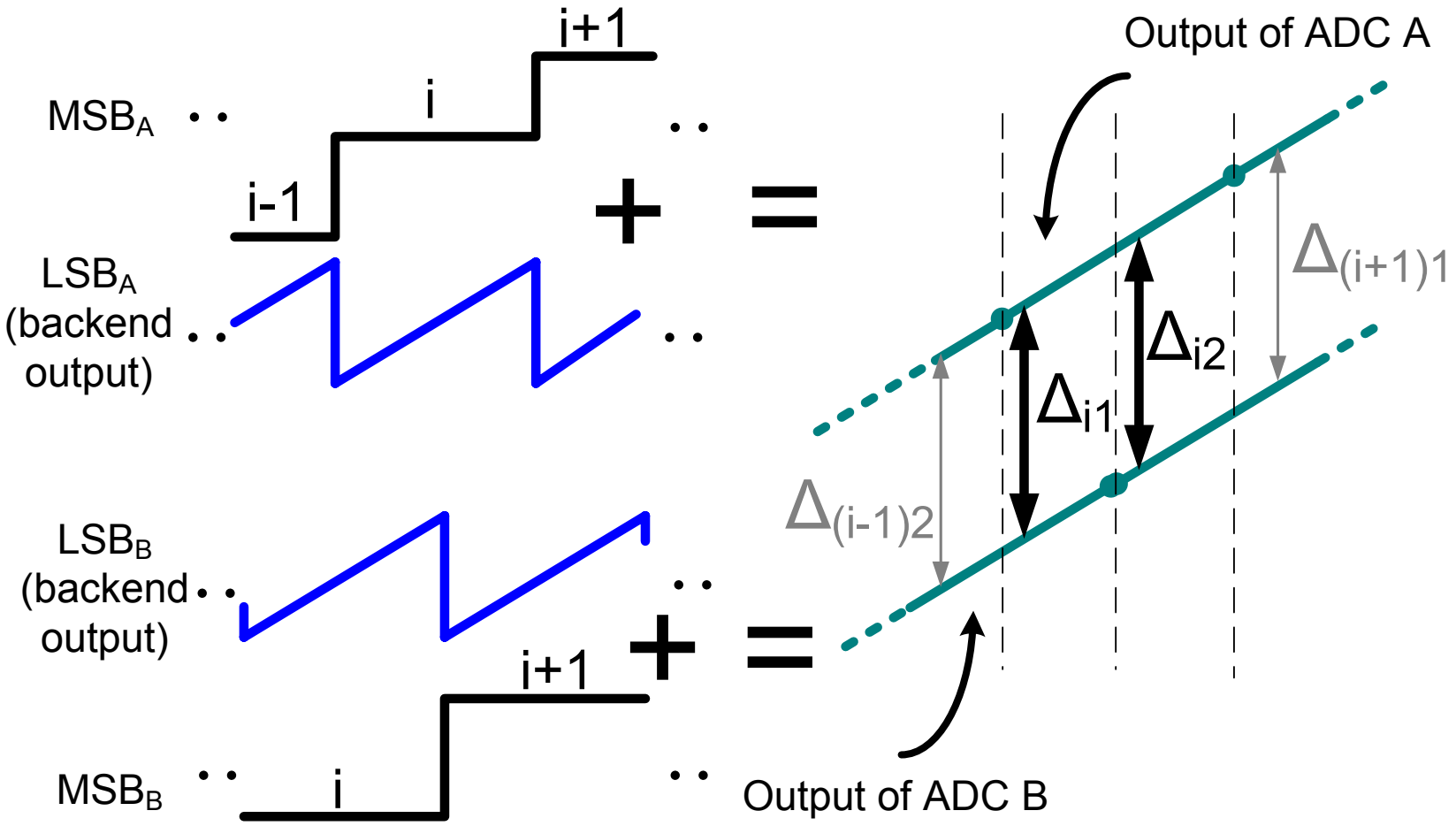


- Gain errors special case of DAC errors → δ(i)= δ
- Thus Correcting DAC errors, also corrects gain errors

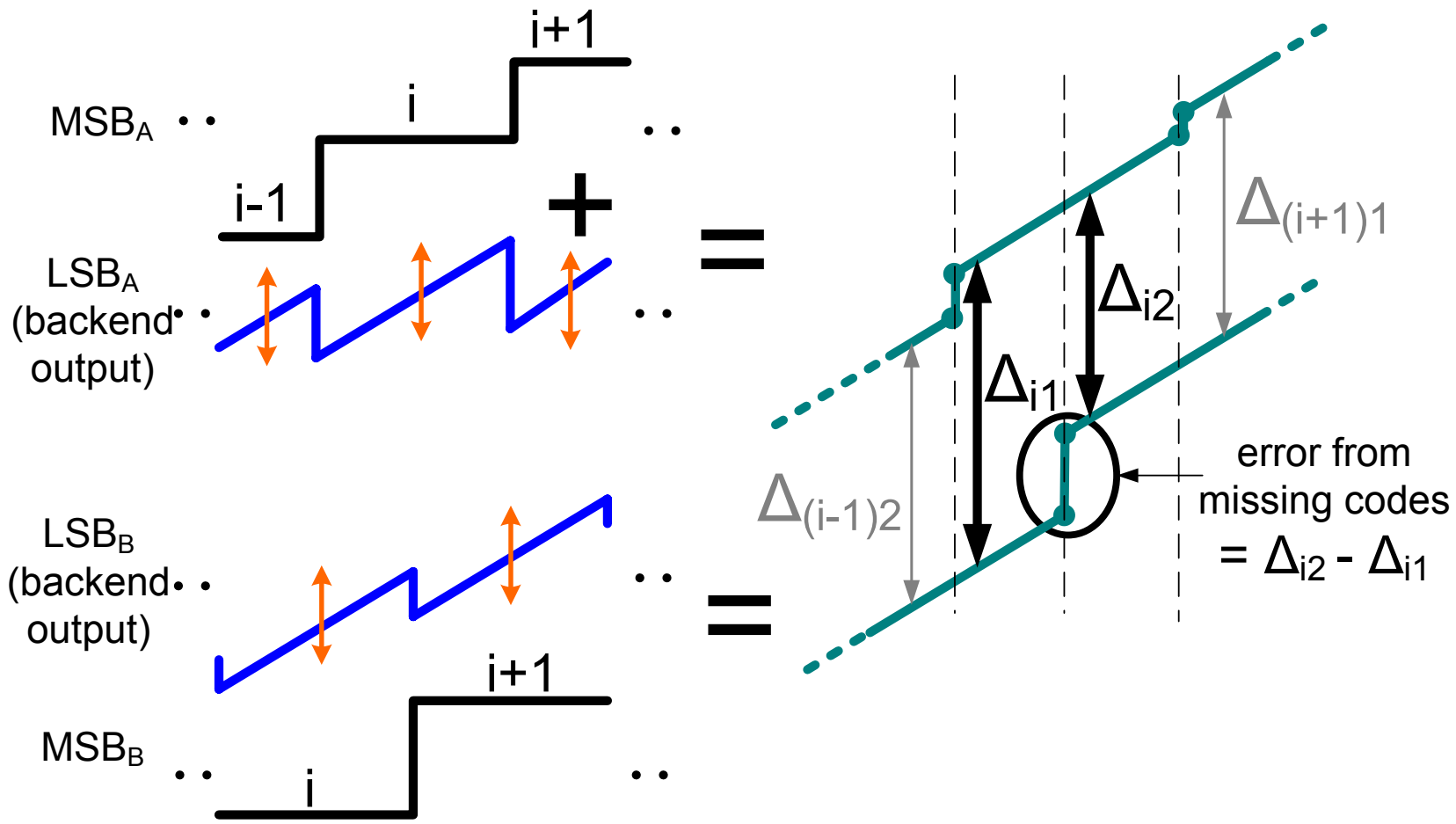
1st stage residues in this work



1st stage residues: no errors

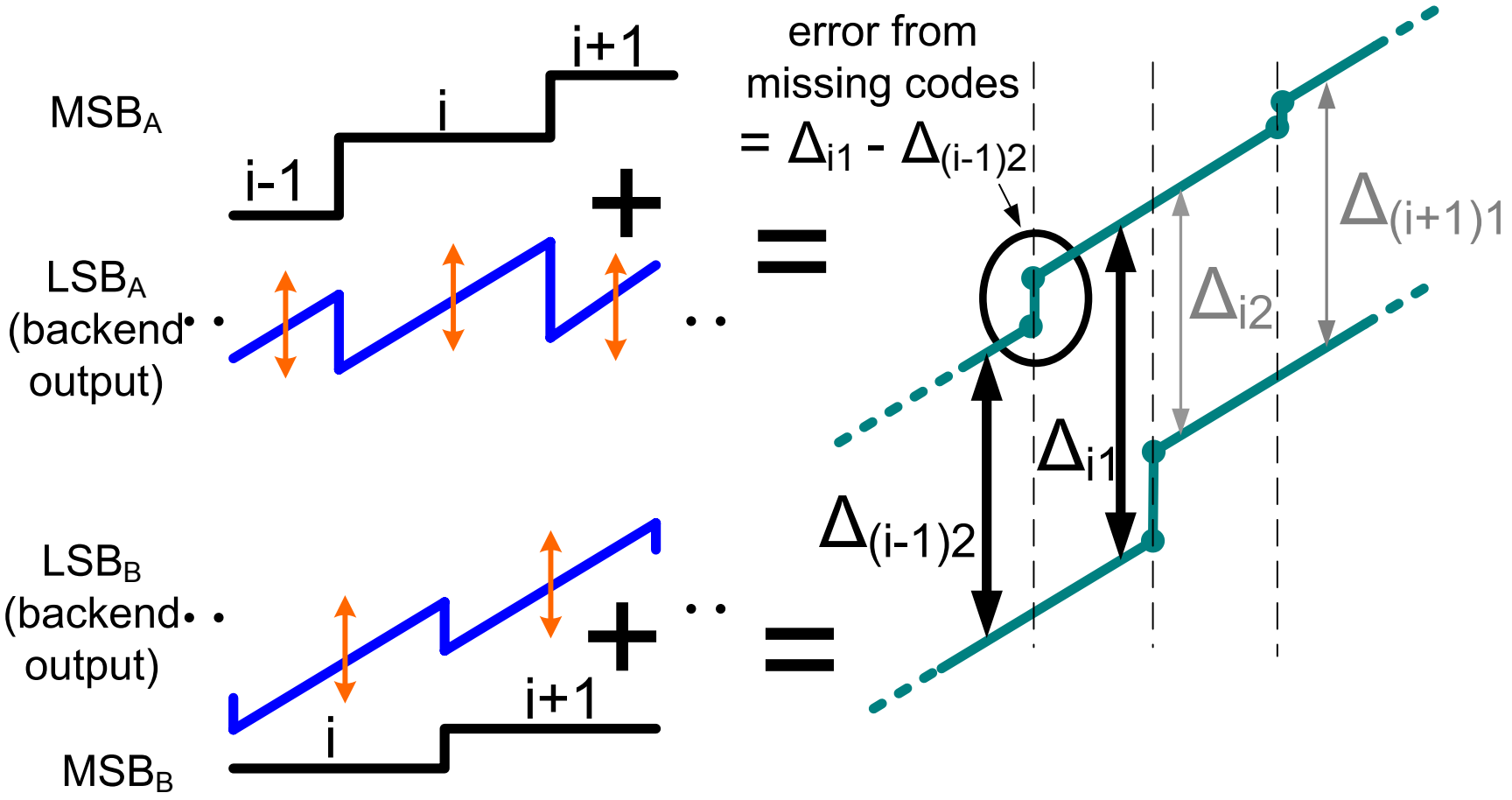


1st stage residues: with DAC errors



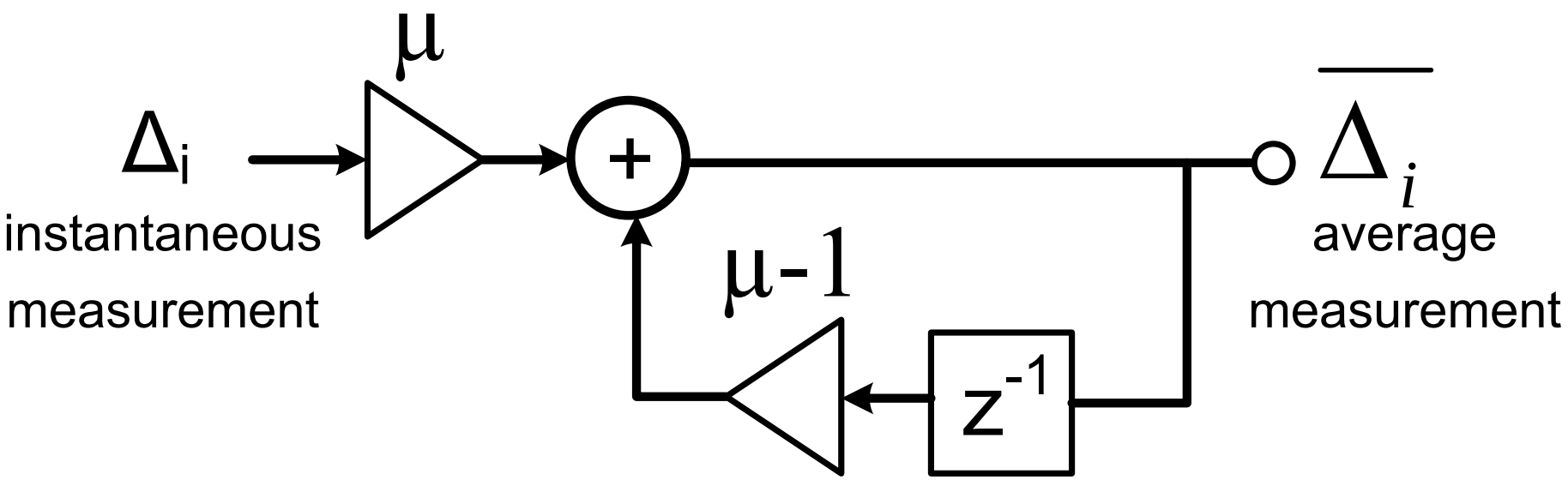
- ADC A used as ideal reference to measure errors of ADC B
- single DAC error measured with minimum of 2 clock cycles

ADC A: error measurement



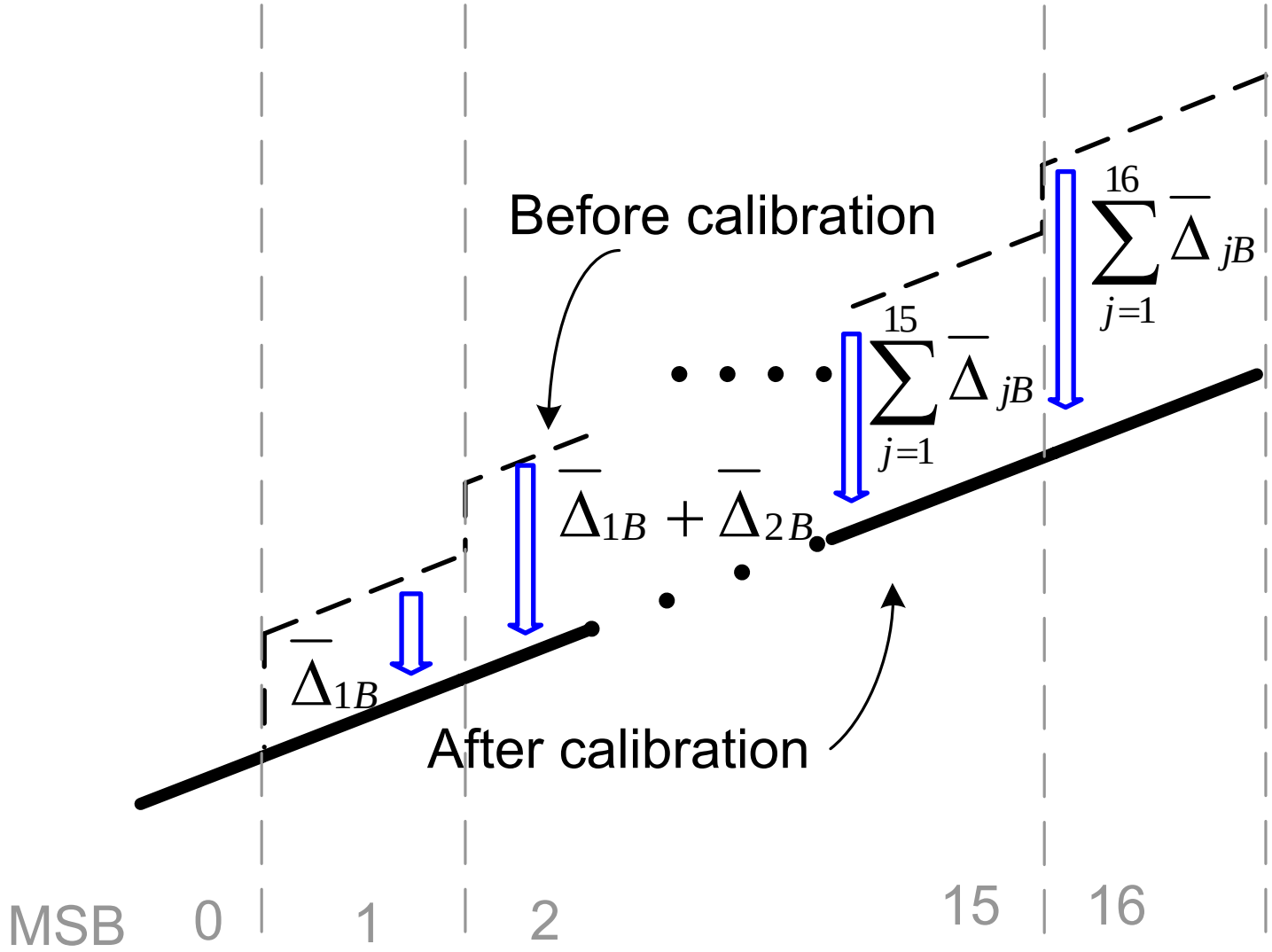
- Calibration requires input to be sufficiently busy to excite each MSB

Digital Error IIR filter

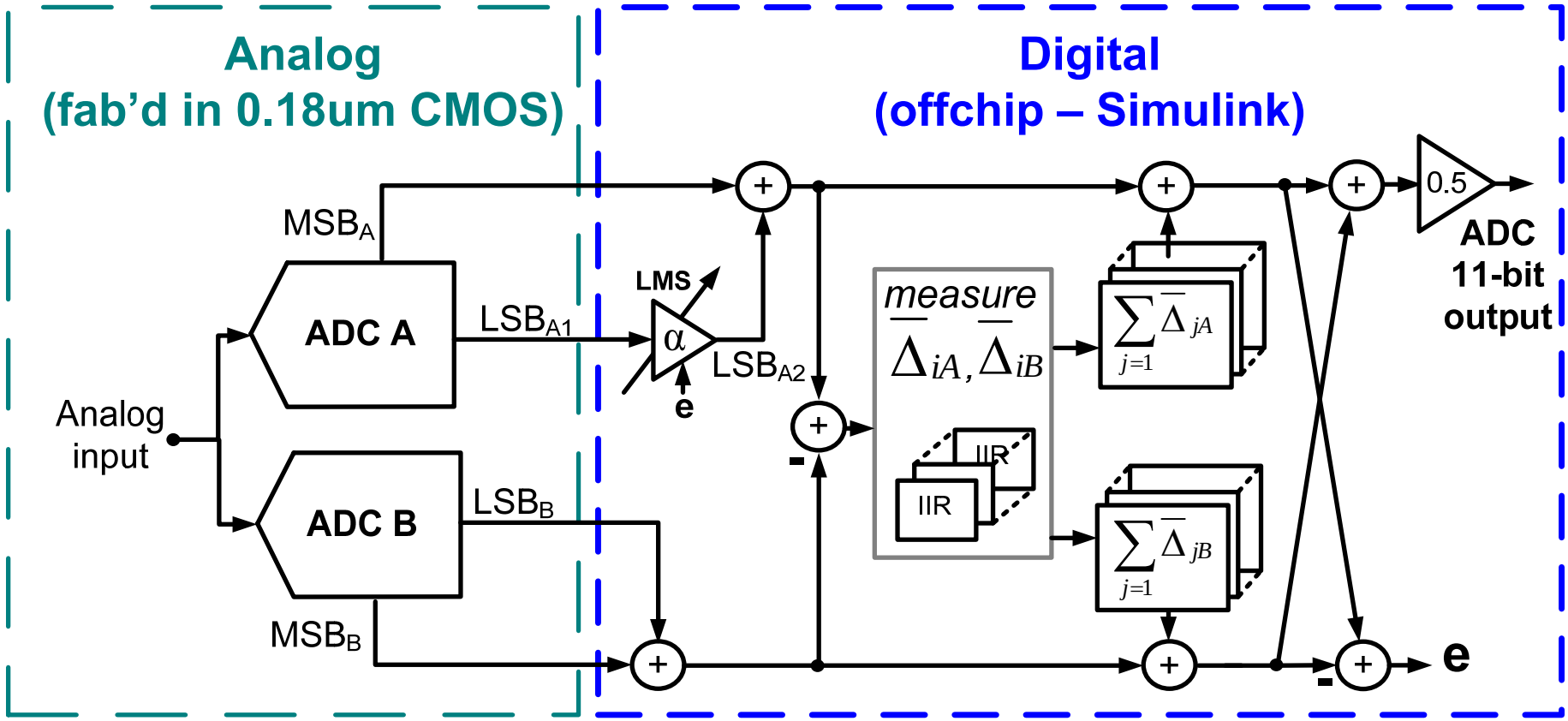


- Use average error to minimize noise and input dependency
- μ a power of 2 for simple implementation

Digital correction of errors

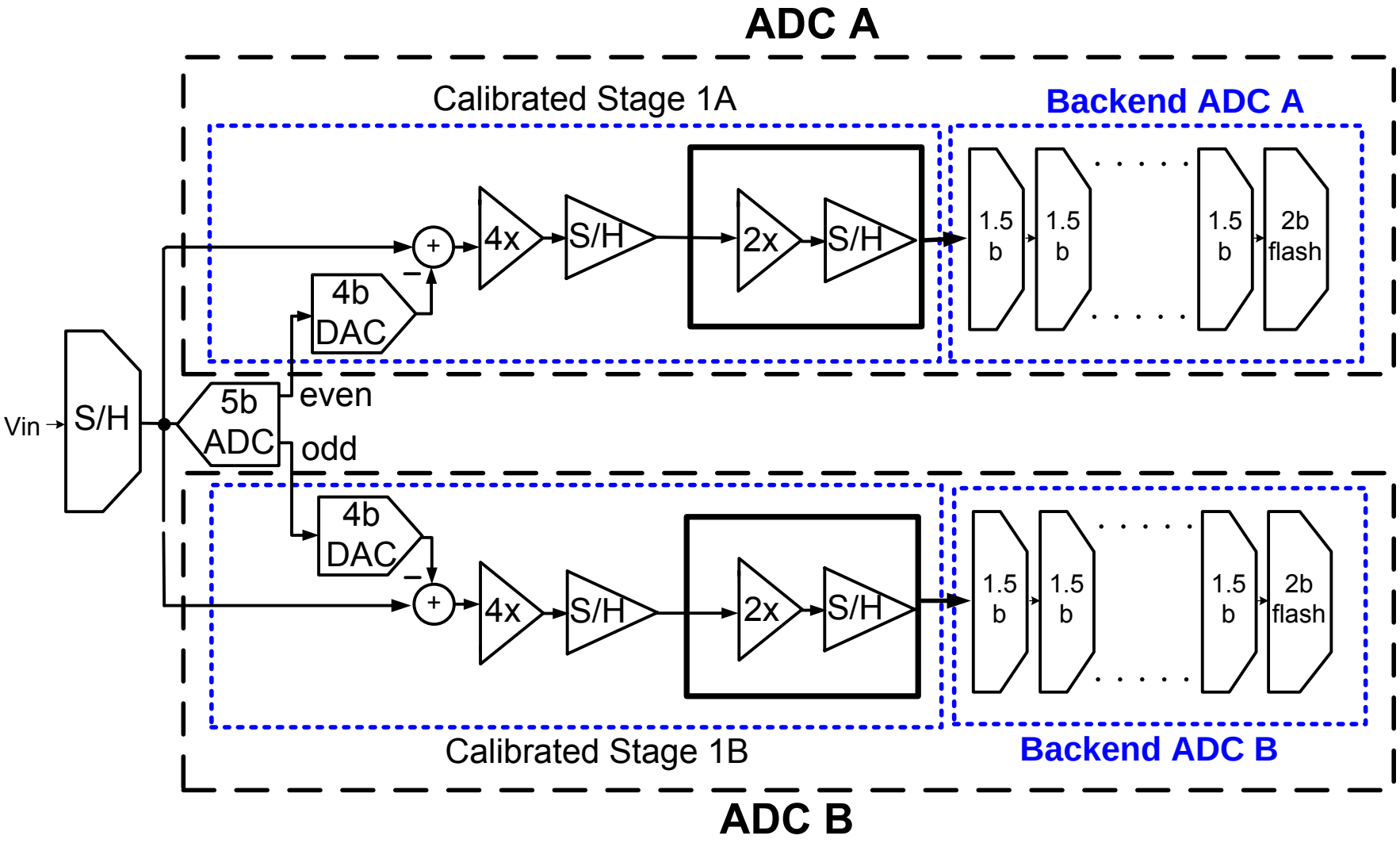


Calibration architecture in full



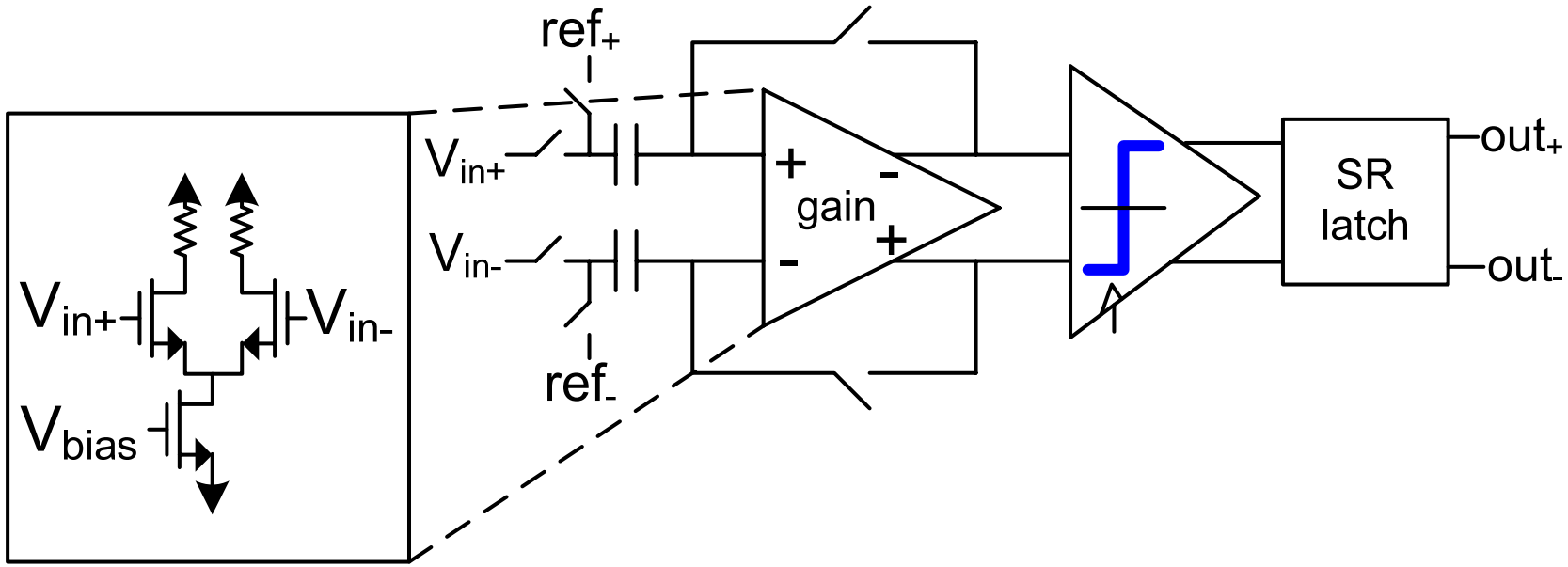
- Include LMS adaptive term α to match ADC gains

Circuit top-level



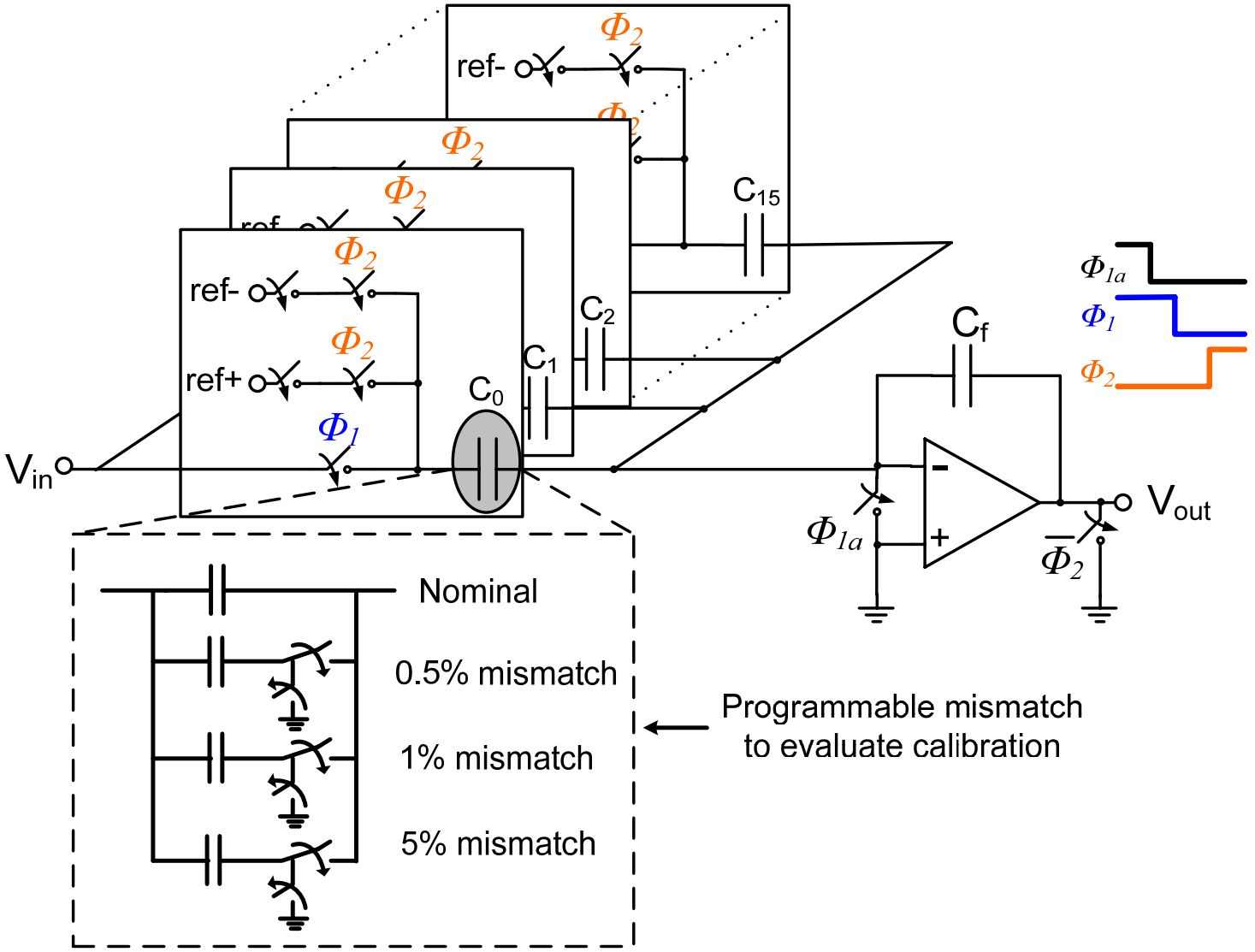
- Gain reduced from 8x to 4x → larger feedback factor

5-bit Flash ADC - comparator

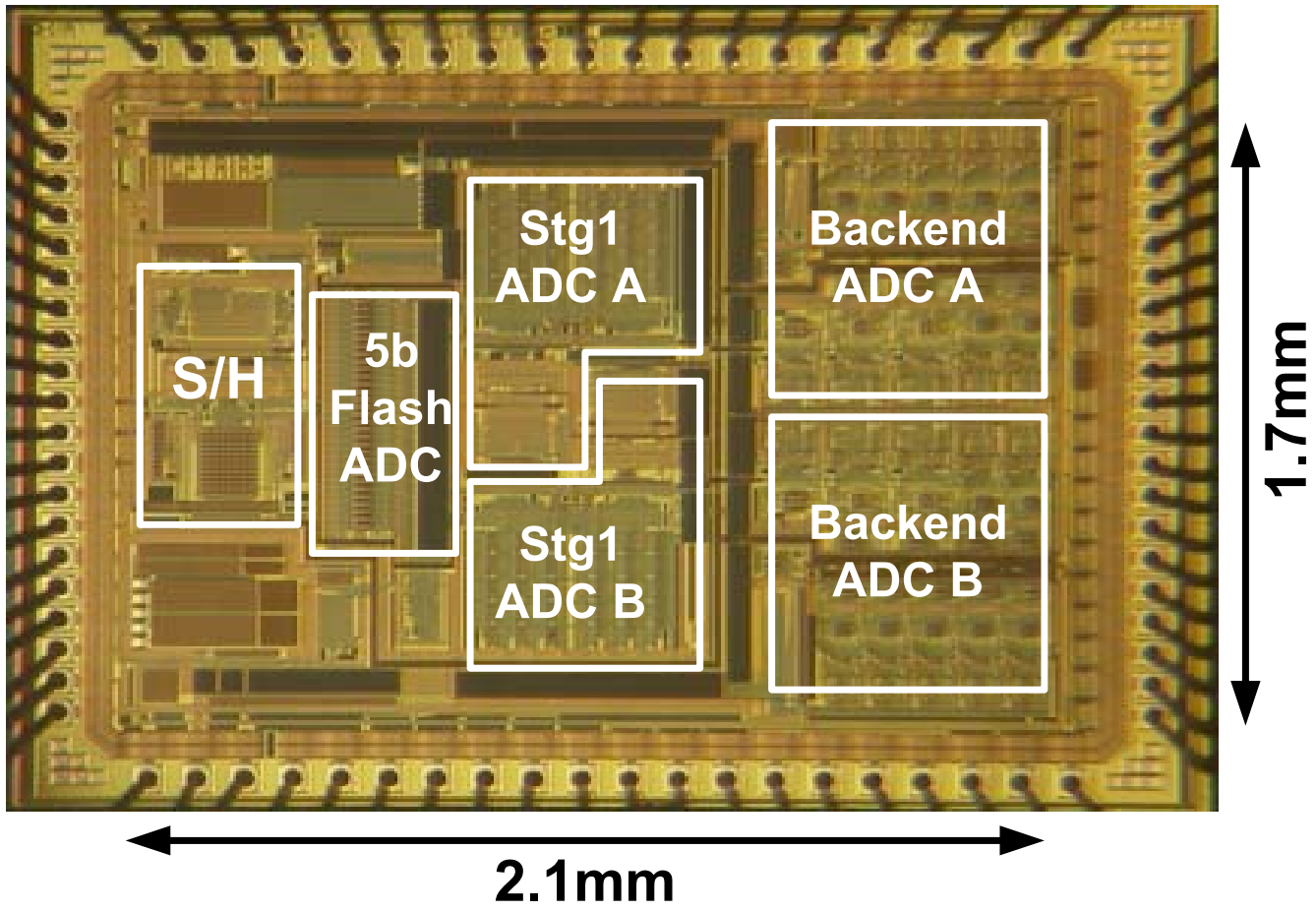


- Array of comparators used for 5-bit flash
- Resistor string used for Flash ADC reference voltages
- Preamp to reduce offset, minimize kickback

Testability: Process variation

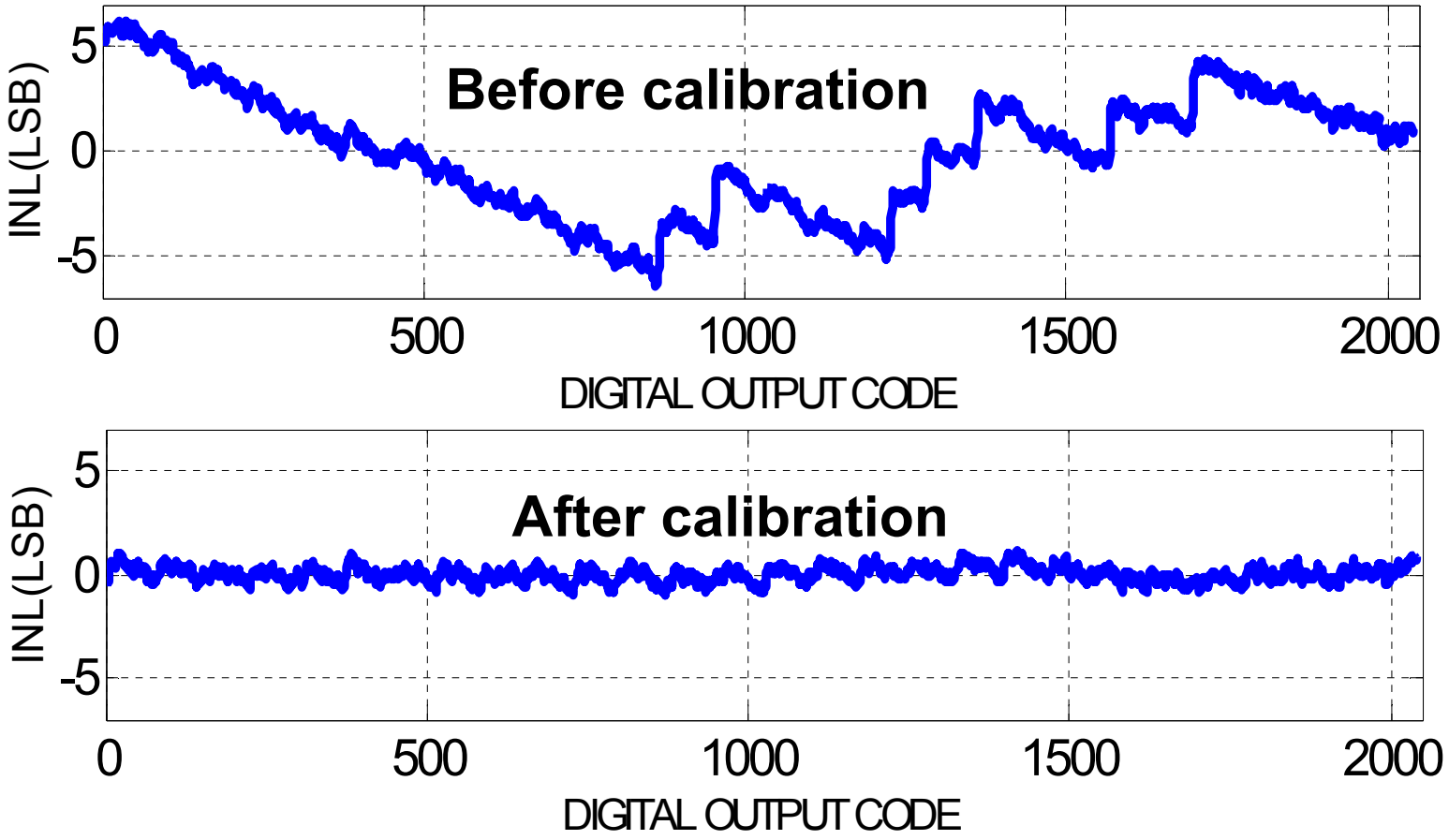


0.18µm CMOS Chip Micrograph



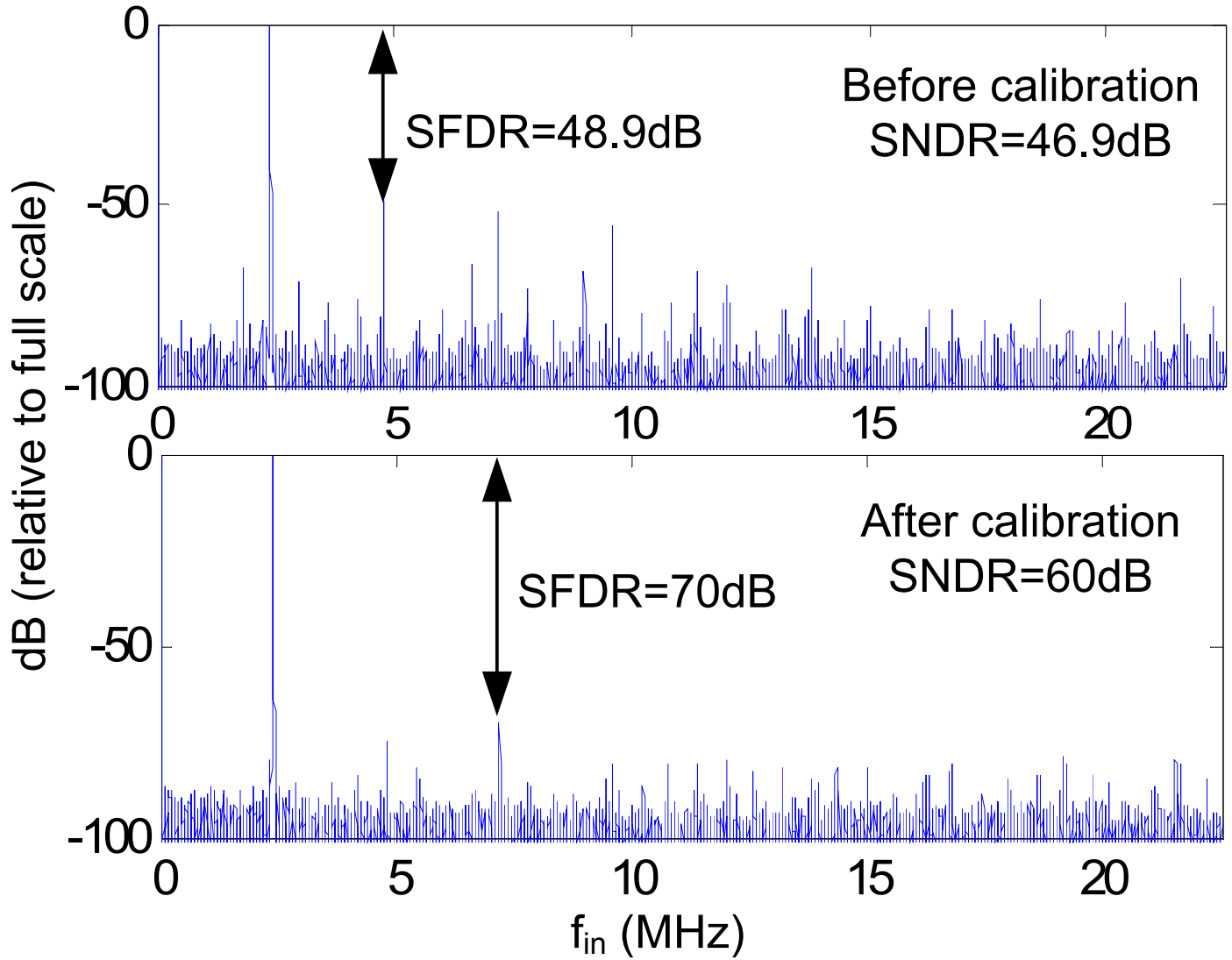
- Area = 3.57mm^2
- Power = 81mW (analog core)

INL

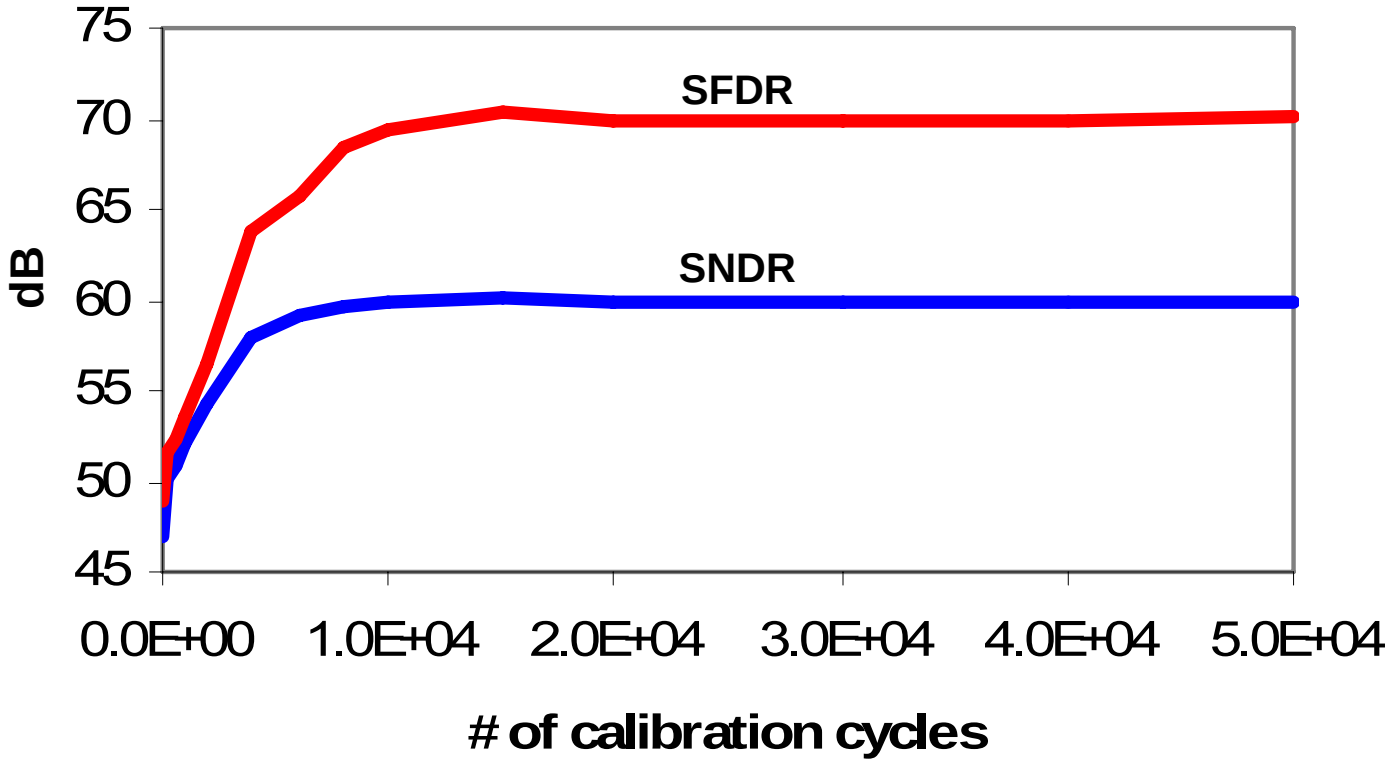


- INL improved from +6.4/-6.1 to +1.1/-1.0 LSB

FFT


0
-50
-100
SFDR=48.9dB
Before calibration
SNDR=46.9dB
0
5
10
15
20
0
-50
-100
SFDR=70dB
After calibration
SNDR=60dB
0
5
10
15
20
dB (relative to full scale)
f_{in} (MHz)

Accuracy improvement over time



- 11-bit linearity within $\mathbf{10^4}$ cycles (i.e. 0.22ms)
- Compare to $2^{2(11)} = 4 \times 10^6$
- Verified with different 'busy' full scale inputs

Performance summary

f_s=45MS/s (f_{in}=2.39MHz)		
	Before calibration	**After Calibration**
INL (LSB)	+6.4/-6.1	+1.1/-1.0
SFDR (dB)	48.9	70
SNDR	46.9	60
Power (analog core)	81mW	
Area	3.57mm^2	
# calibration cycles	10^4 cycles, (0.22ms)	

Conclusions

- Presented architecture to rapidly correct DAC and gain errors in multi-bit pipeline stage
- Measured results in 0.18μm CMOS show linearity improved by >3b within 10^4 clock cycles
- Calibration achieved in more than **two order of magnitude fewer clock cycles** than prior statistical approaches

Acknowledgements

- Feedback from Professor Ken Martin, *University of Toronto*

- The generous funding from the National Sciences and Research Council of Canada (NSERC)

- The fabrication services of the Canadian Microelectronic Corporation (CMC)