ESSCIRC 2007
Session A3L-G4

A high bandwidth power scaleable sub-sampling 10-bit pipelined ADC with embedded sample and hold

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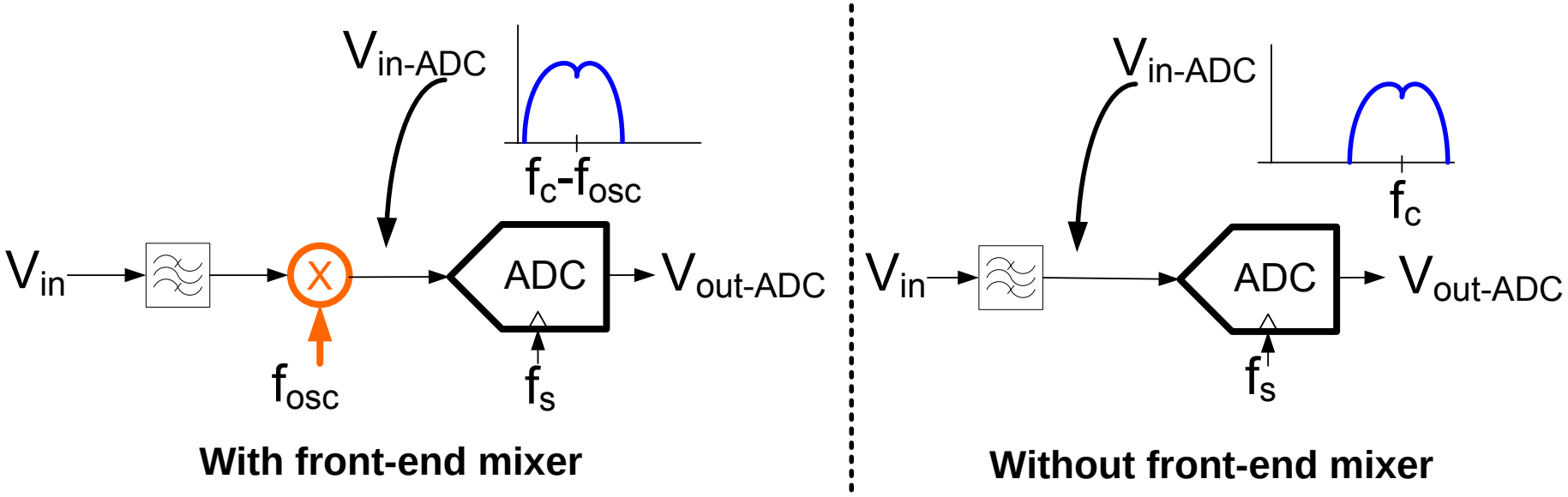
Overview

- Motivations
- State of the art
- Approach of this work
  - Technique to remove front-end S/H
    - Works for very high input frequencies
  - Design in 0.18µm CMOS
- Measurement results
- Summary

Motivations: Sub-sampling



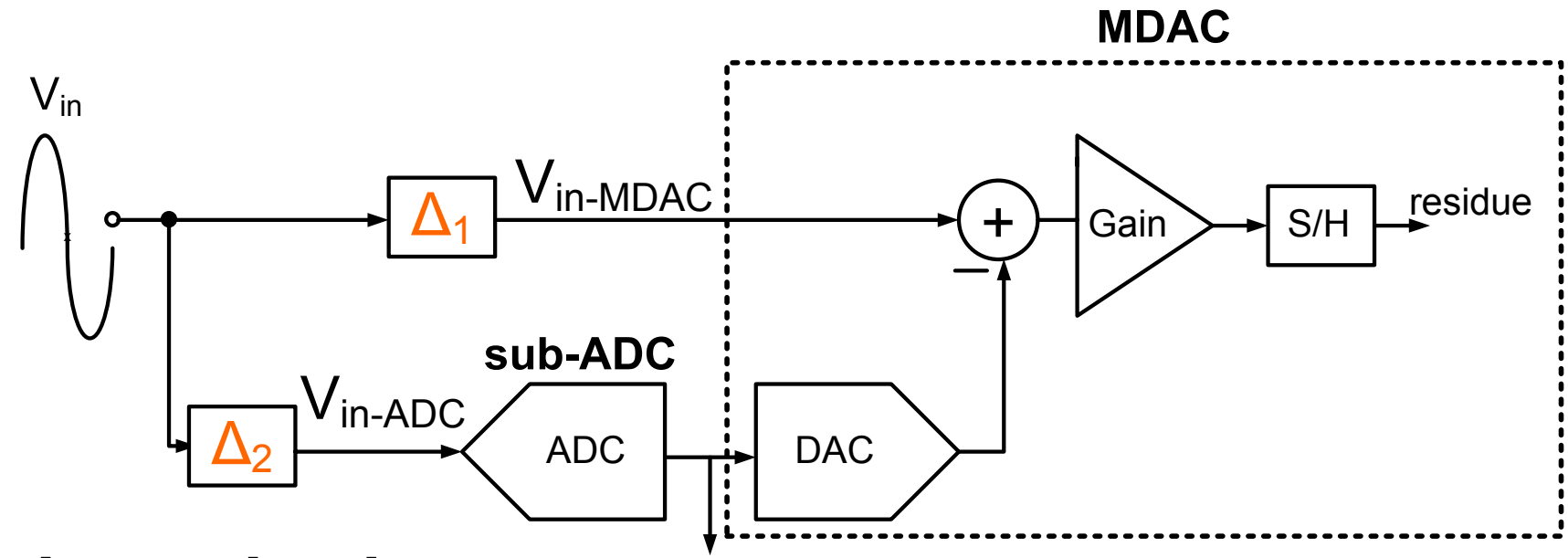
Remove input mixer in IF systems

- √ Saves power
- X Significantly increases ADC input bandwidth

Power scaleable ADC for IF applications

- ADC can be used for variety of applications with minimal power
- E.g. Multi-Standard, Multirate

large input BW in pipelined ADCs

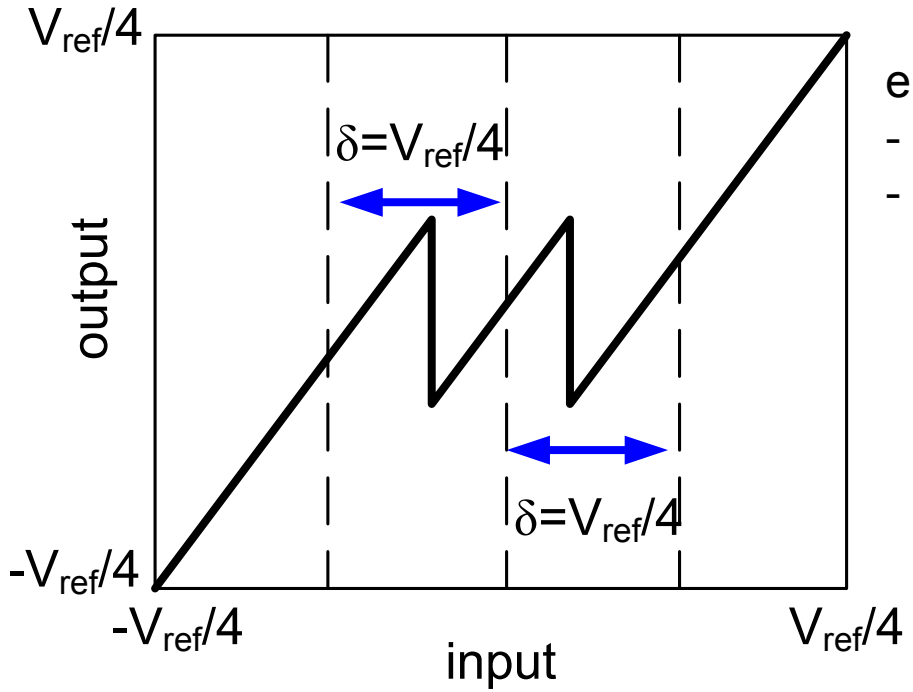


$\Delta_{skew} = \Delta_1 - \Delta_2$

$V_{in\text{-}MDAC} \neq V_{in\text{-}ADC}$

- Prior works use power hungry front-end S/H to ensure MDAC, sub-ADC inputs are the same

S/H removal: prior art



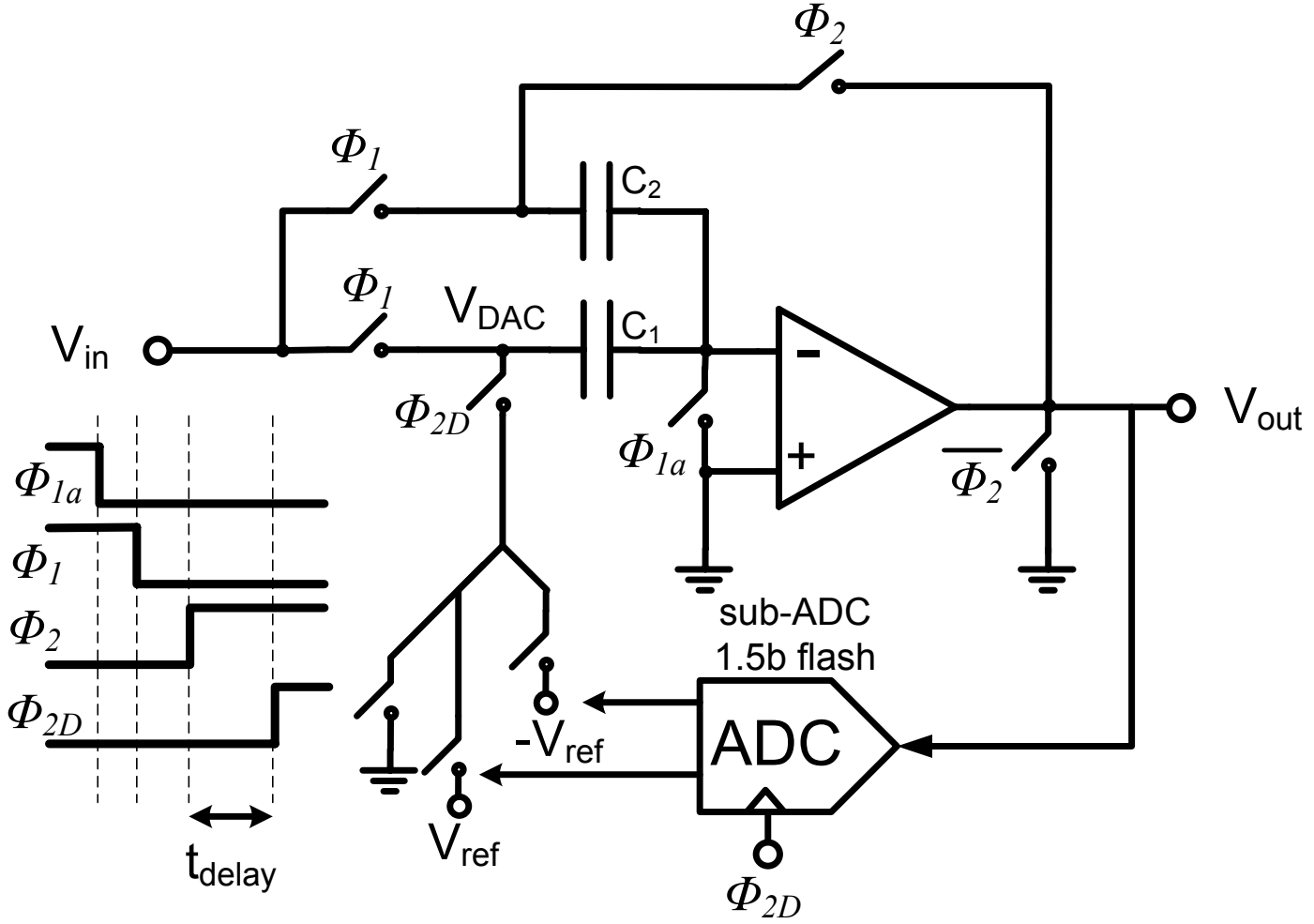
e.g. references
- [Gulati et al, JSSC Aug '06]
- [A.A. Ali et al, JSSC Aug '06]

If $|V_{in\text{-}MDAC} - V_{in\text{-}ADC}| < \delta \rightarrow$ no error

True if $|\Delta_{skew}| < \frac{1}{8\pi f_{in}}$ for 1.5b stage

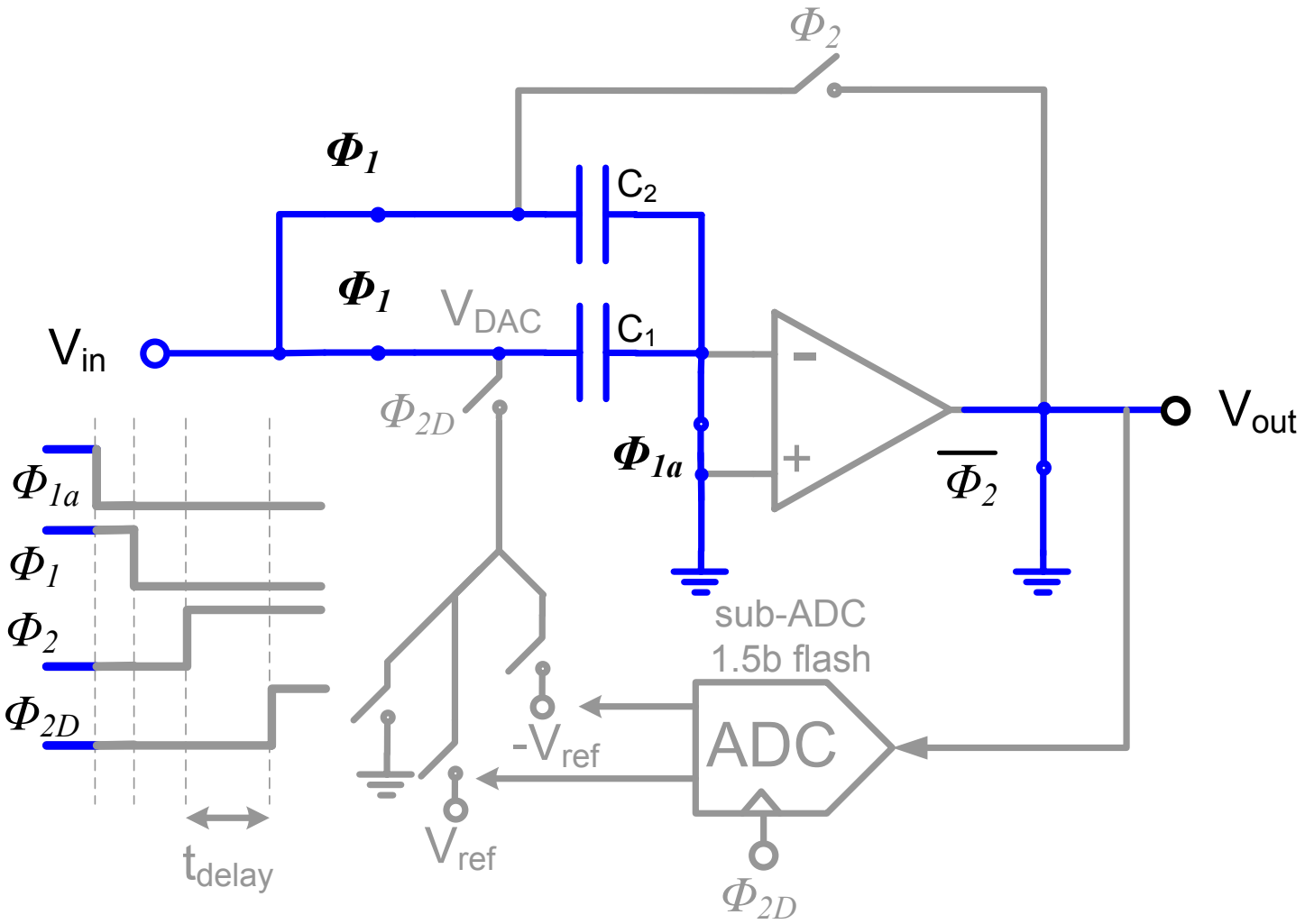
for f_{in}=270MHz, skew < 140ps → need very careful layout to guarantee maximum skew

This work: MDAC w/embedded S/H

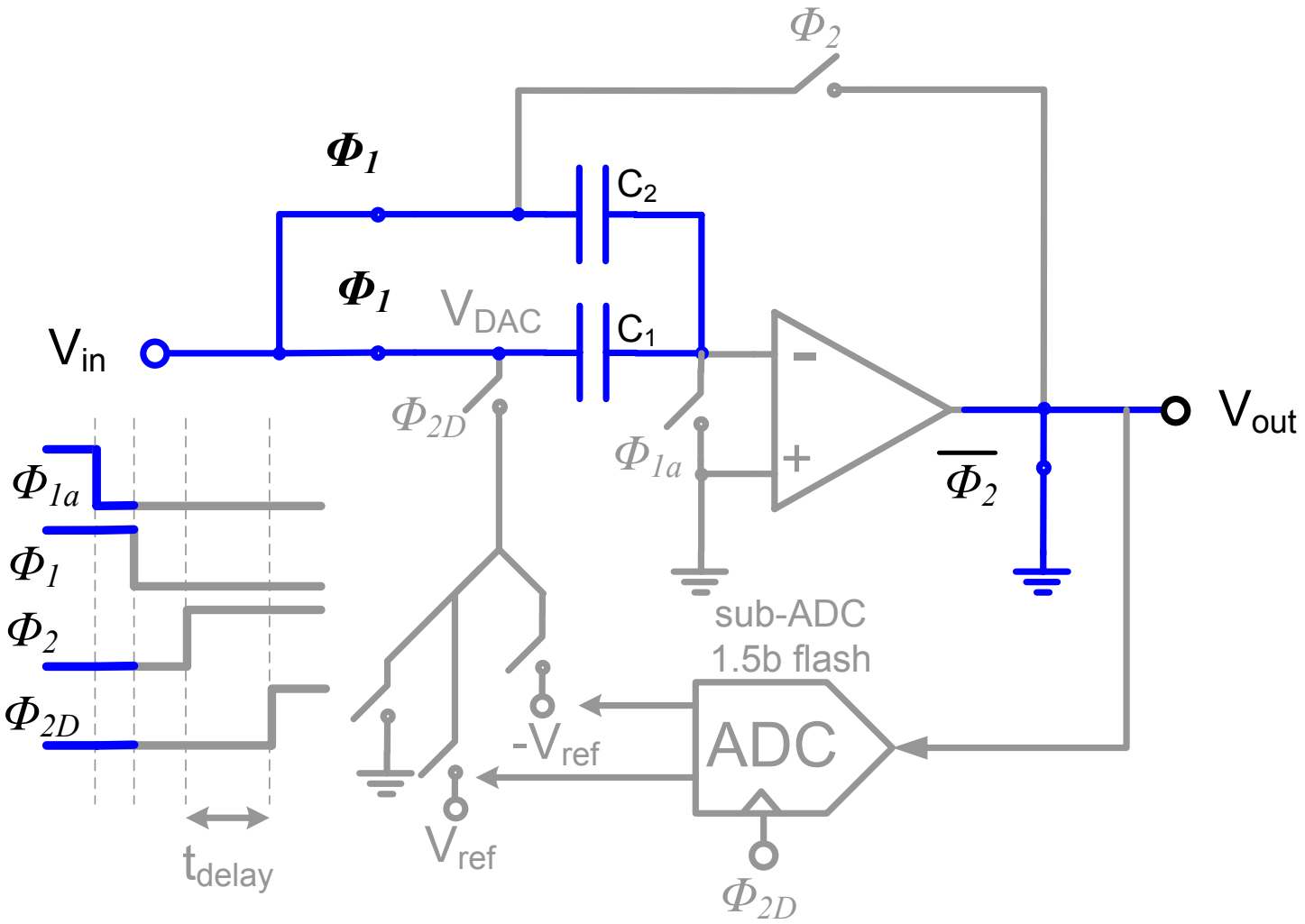


- No front end Sample and Hold required to guarantee sub-ADC, MDAC operate on same input

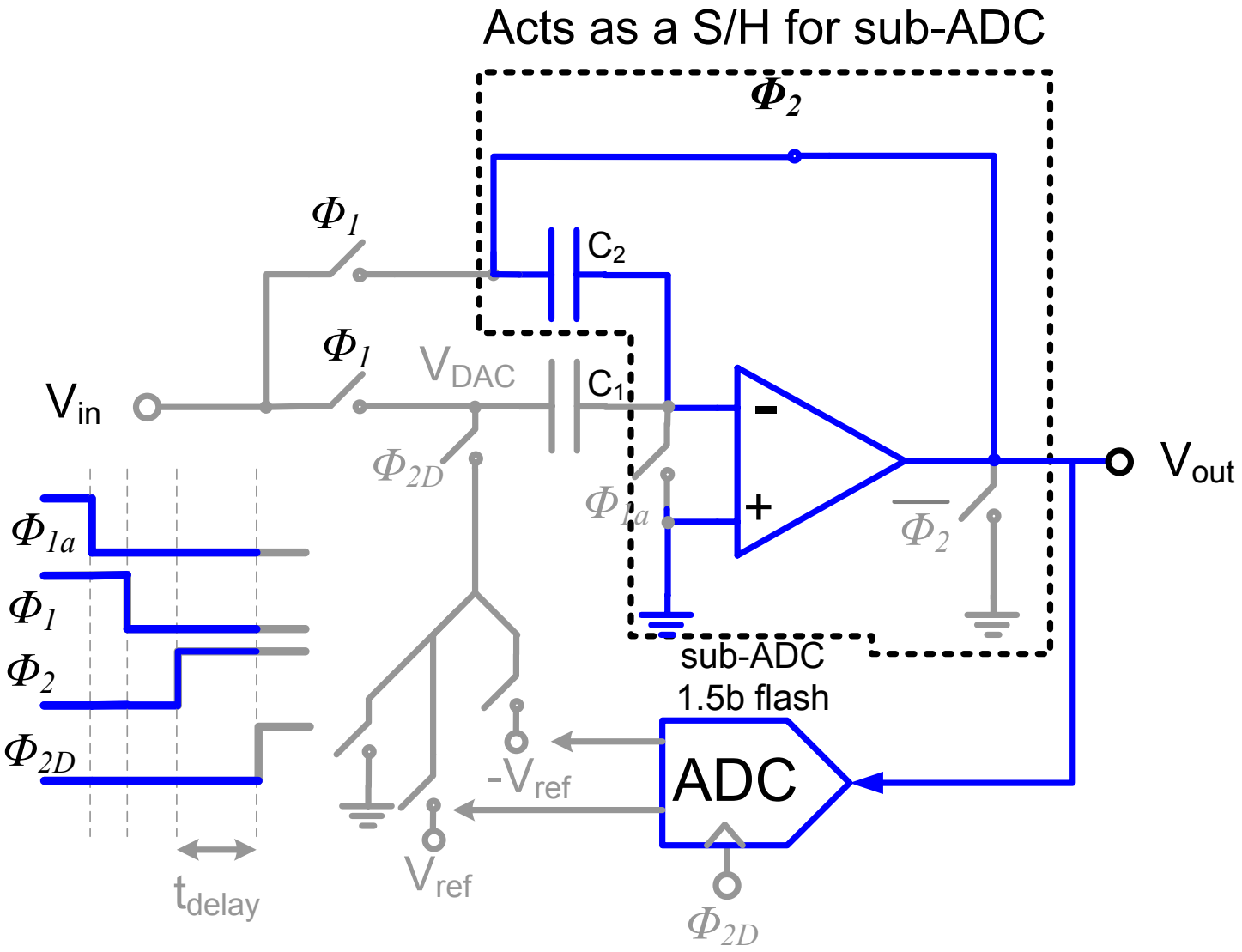
Φ_{1a} – track input



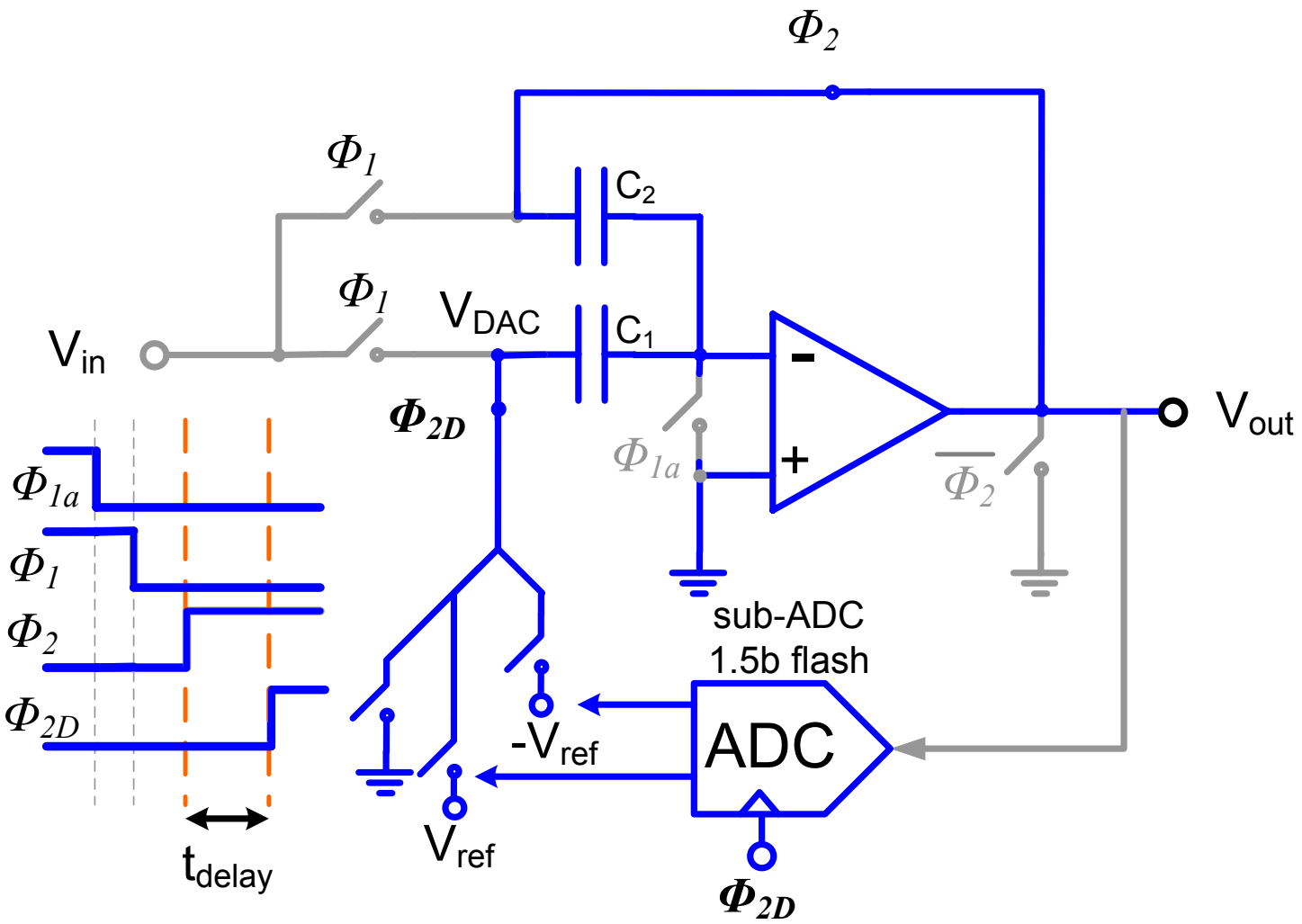
Φ_1 – sample input



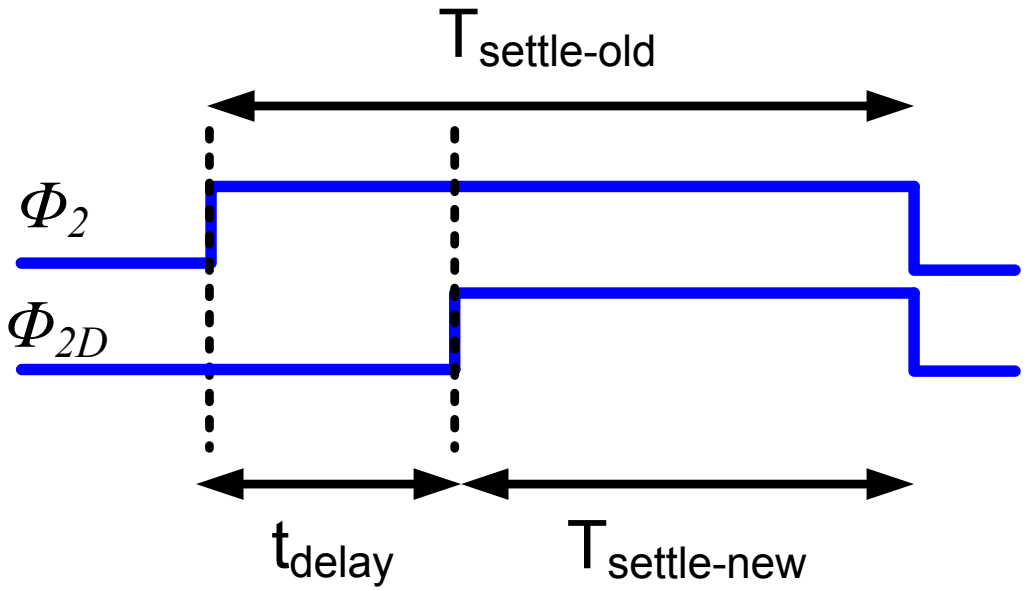
Φ_2 – embedded S/H drives sub-ADC



Φ_{2D} – DAC + gain operation

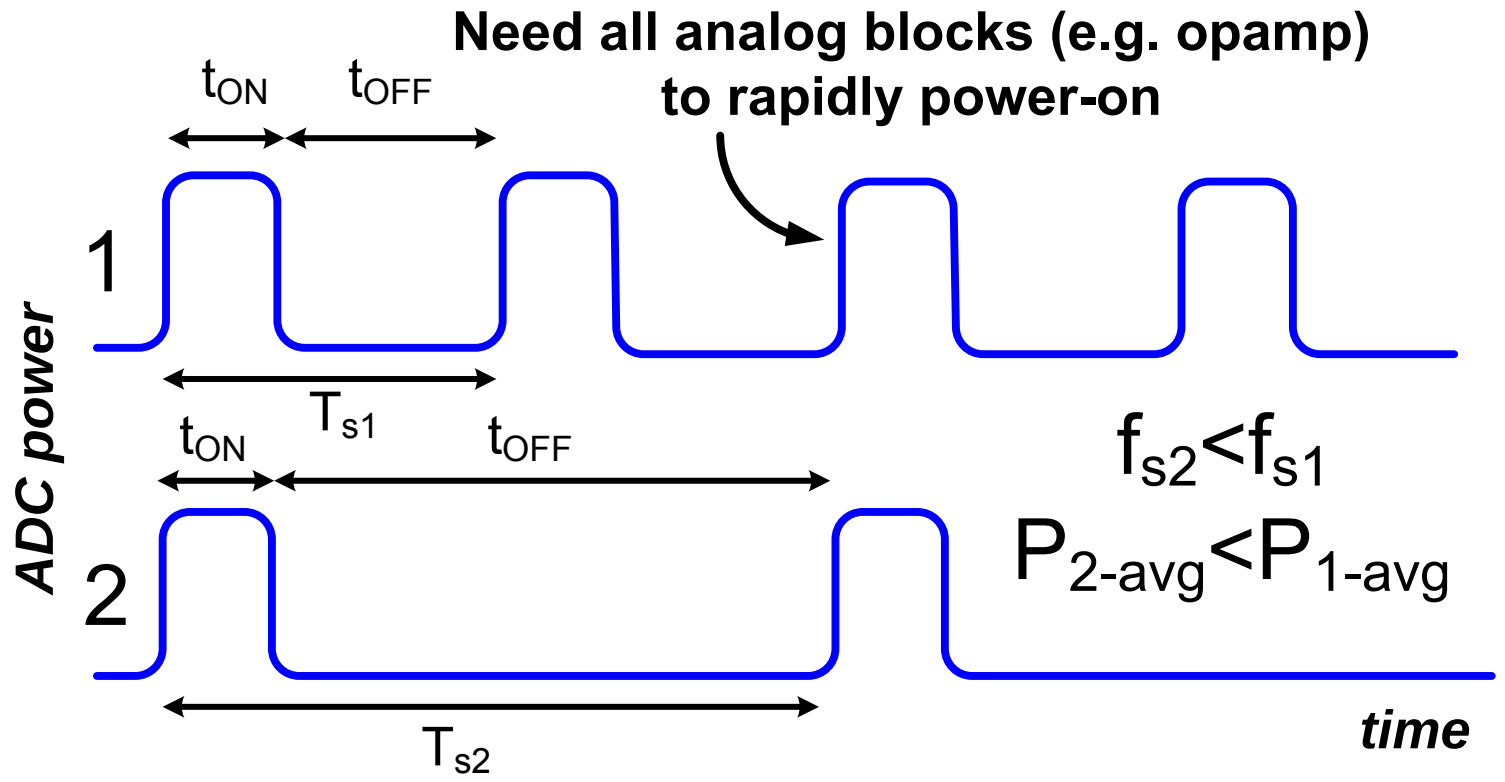


Key observations



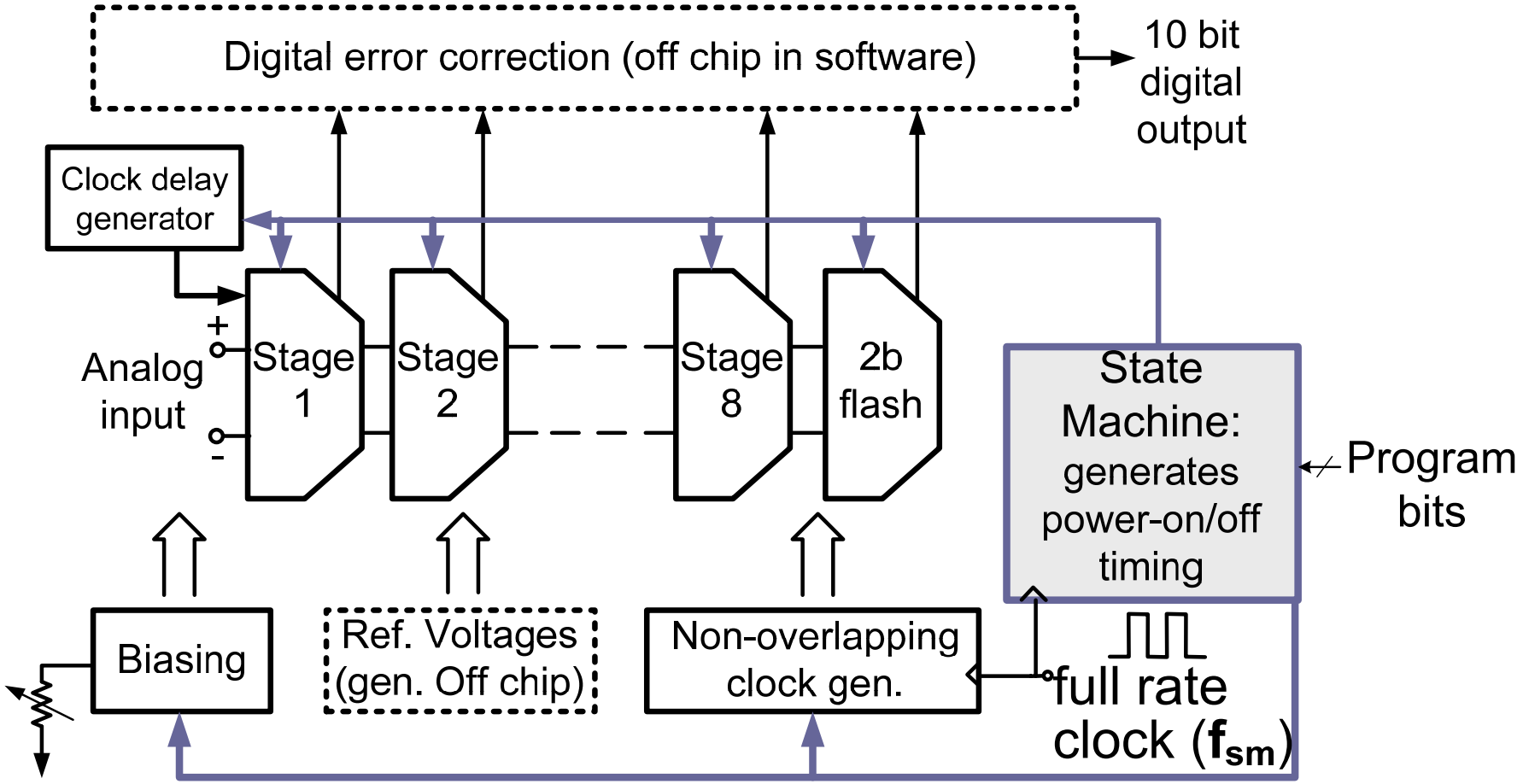
- Settling time of first pipeline stage slightly reduced
  - **front-end S/H eliminated overall power still reduced**
- Technique independently developed, but similar to [Li et al, CICC ’06]
  - This work:
    - 4x larger input bandwidth
    - Power scaleable architecture
    - 66% increase in sampling rate

Power scalability

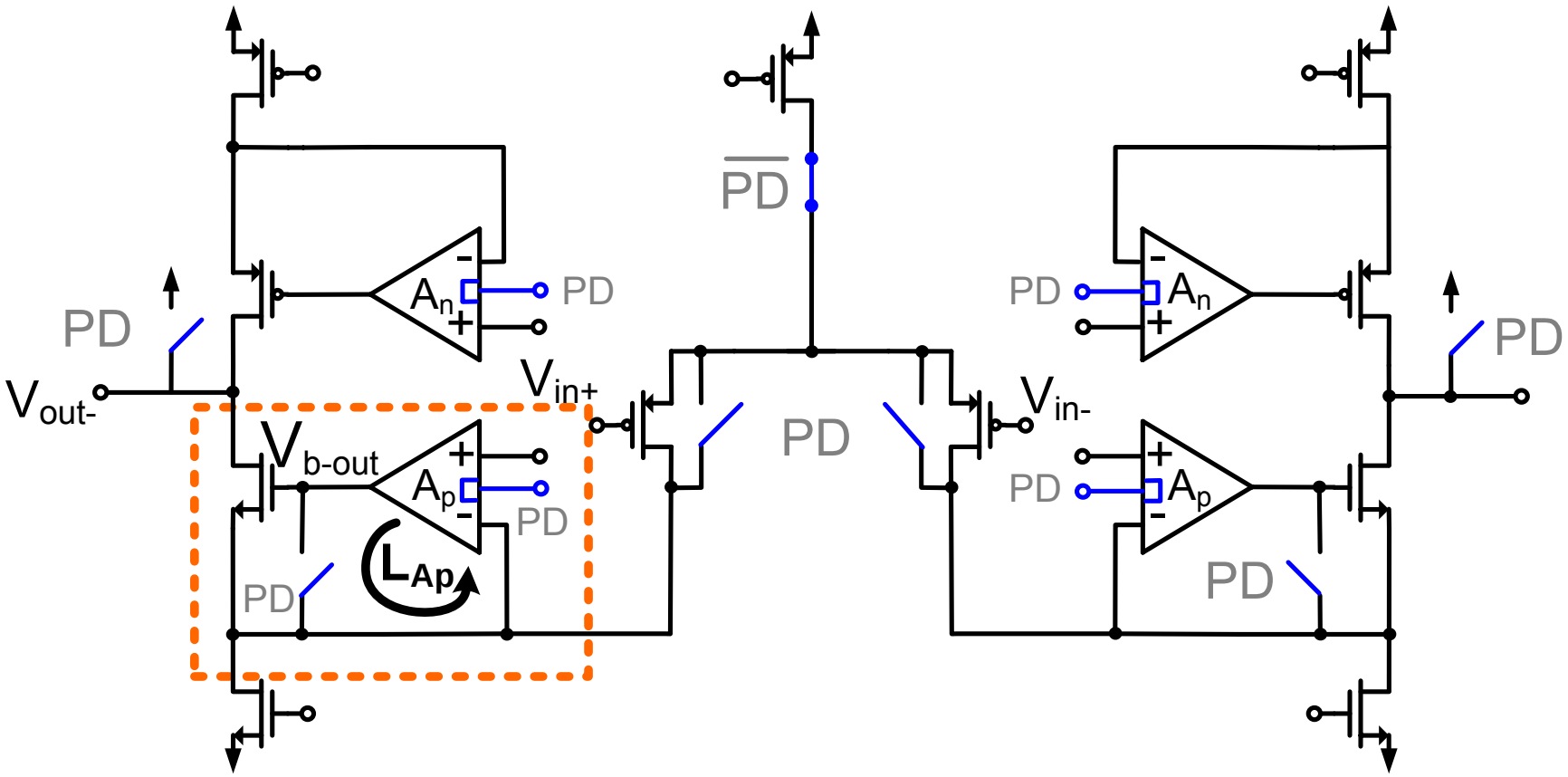


- described in detail in [Ahmed, Johns, JSSC Dec '05]
- scale power with sampling rate over large sampling rate range without large current variations

10b Pipelined ADC architecture

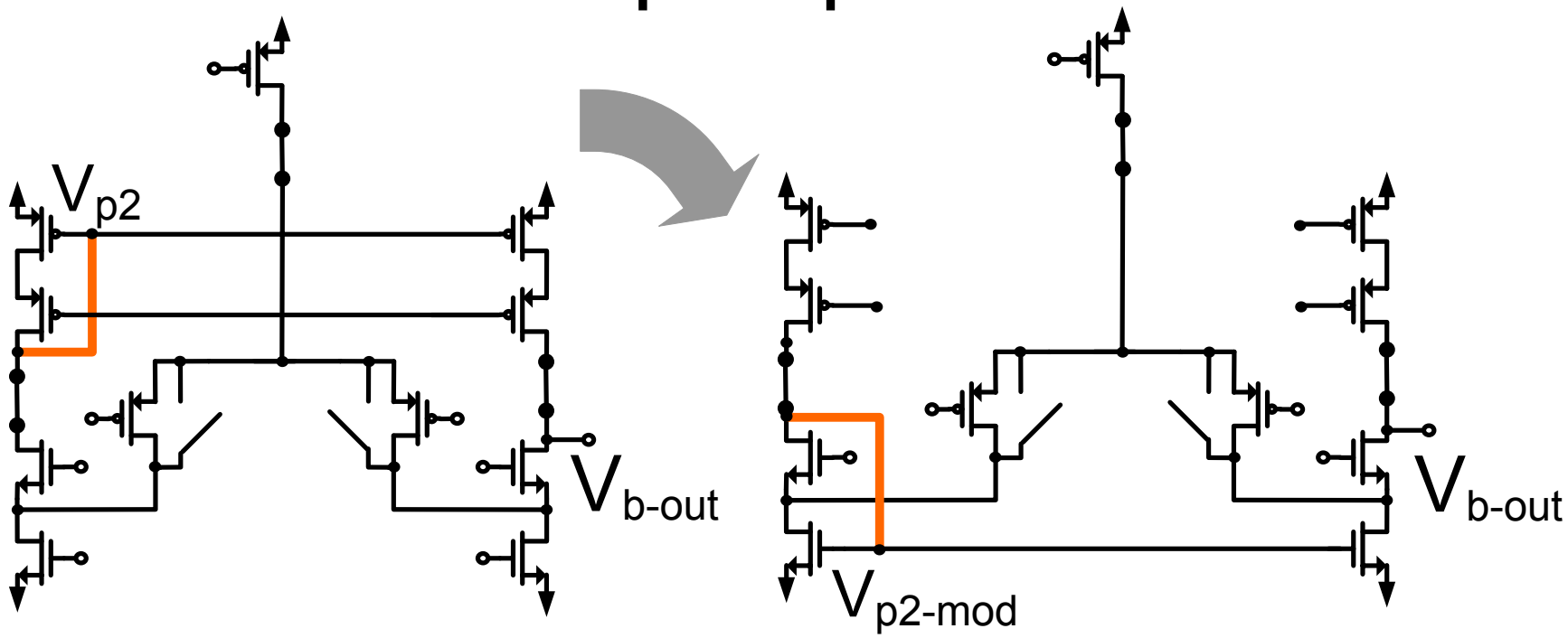


Rapid Power-on Opamp



- Opamp wake-up → gain boosters have step response
- Stable response → large PM for gain booster loop

Stability improvement: gain booster opamp

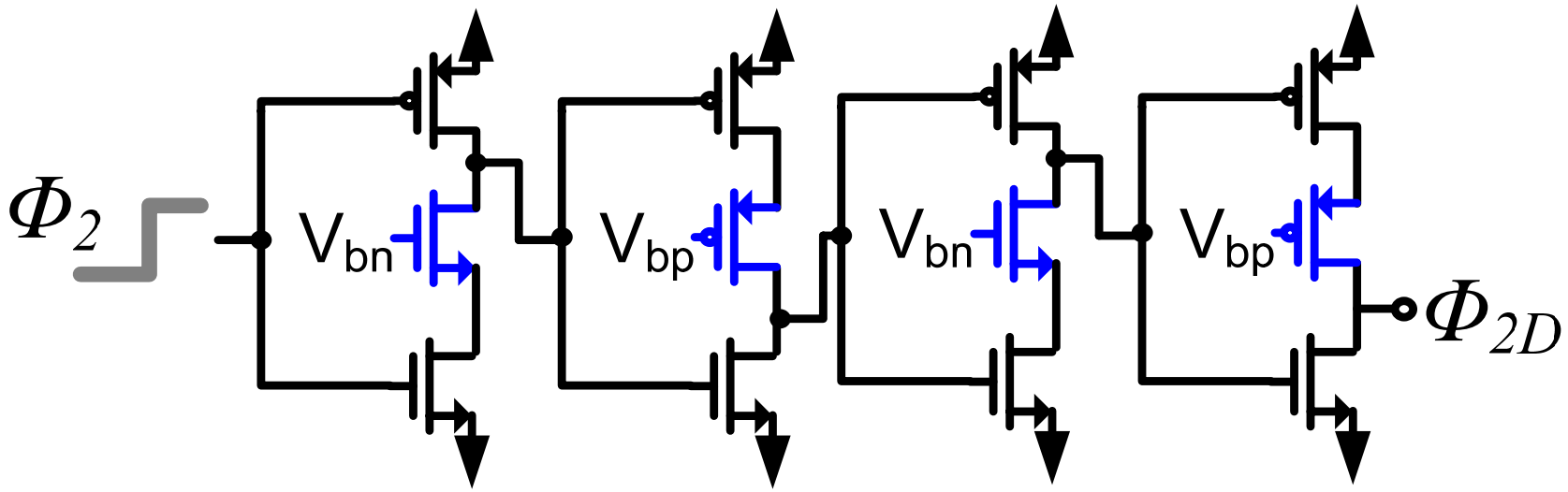


Prior approach
2^{nd} pole set by large PMOS transistors

This work
2^{nd} pole set by smaller NMOS transistors

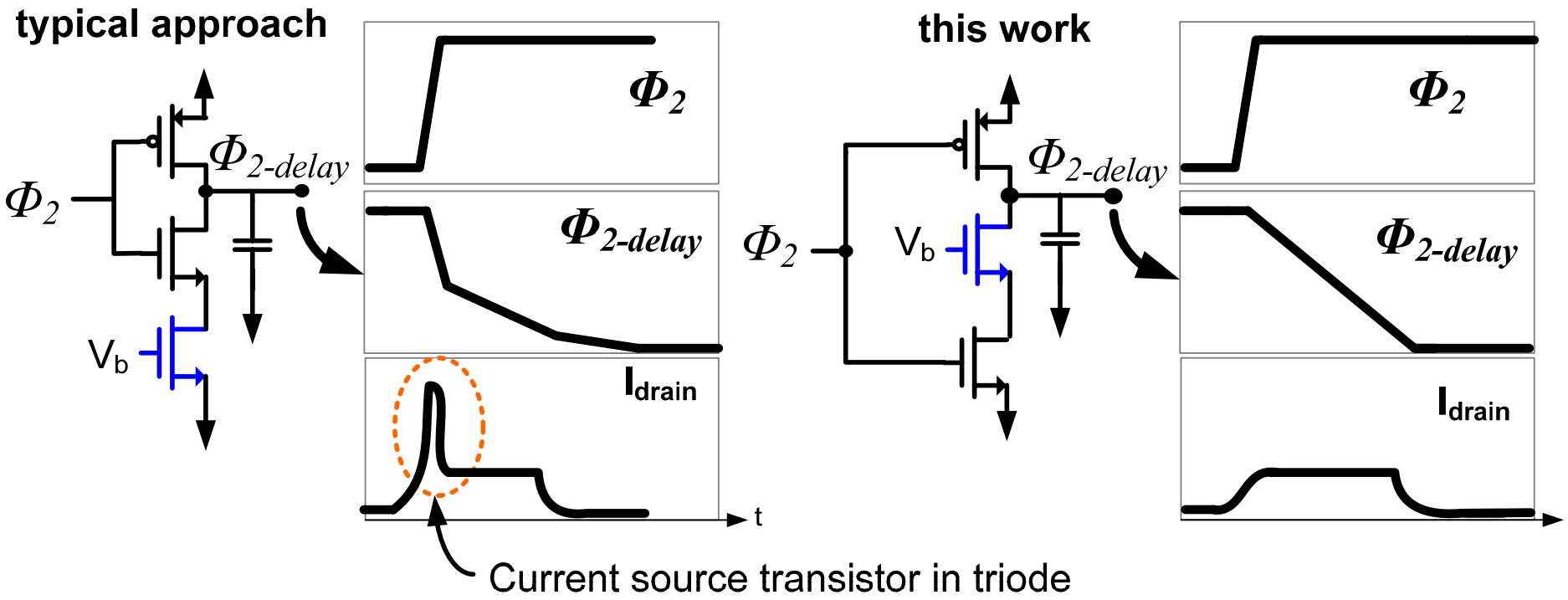
- [Baker: CMOS Circuit Design, Layout and simulation]
- Gain-booster opamp tradeoff: stability vs. slew-rate

Clock delay generator



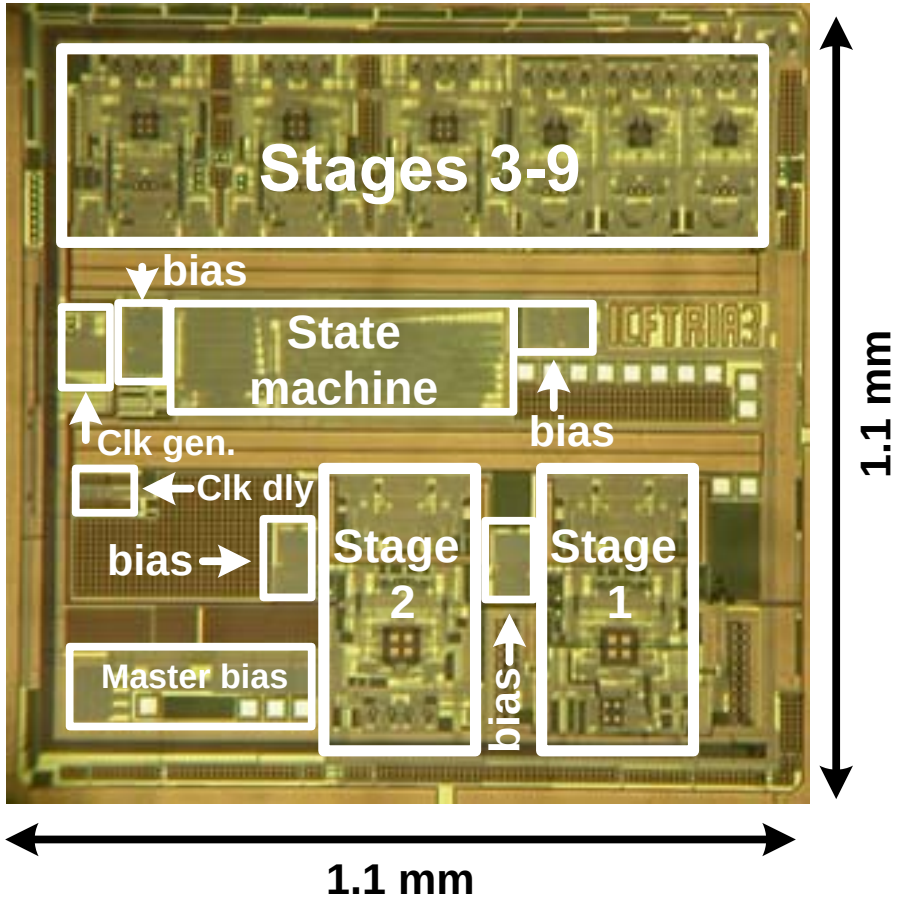
- Require delay to be scaleable for different sampling rates scaleable sampling + validating impact of different delays

Current starved cell: delay control



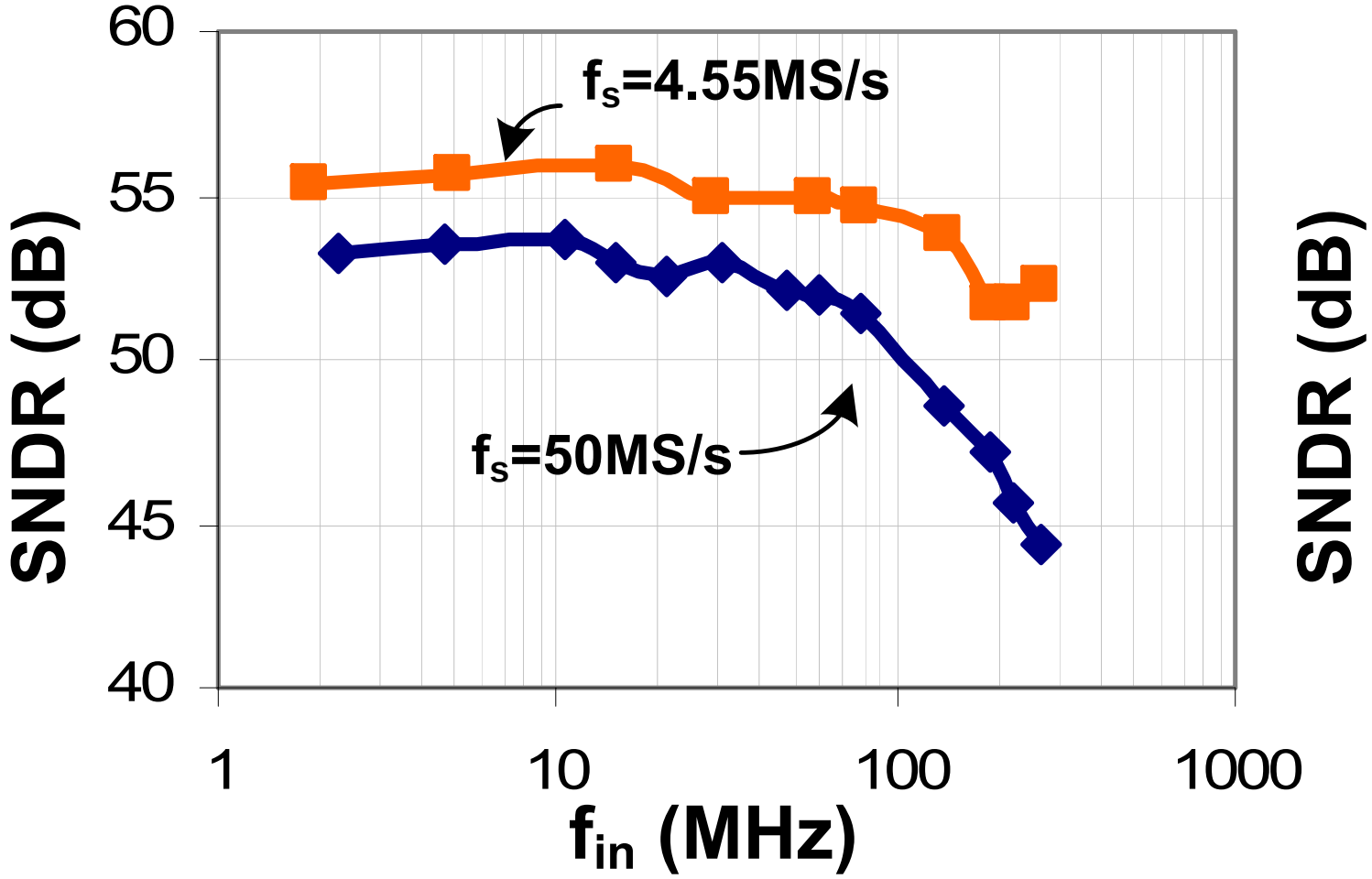
- In this work bias transistor does not enter triode
  - → Delay strong function of bias current
  - → Can scale delay over wide range by scaling current

Chip micrograph

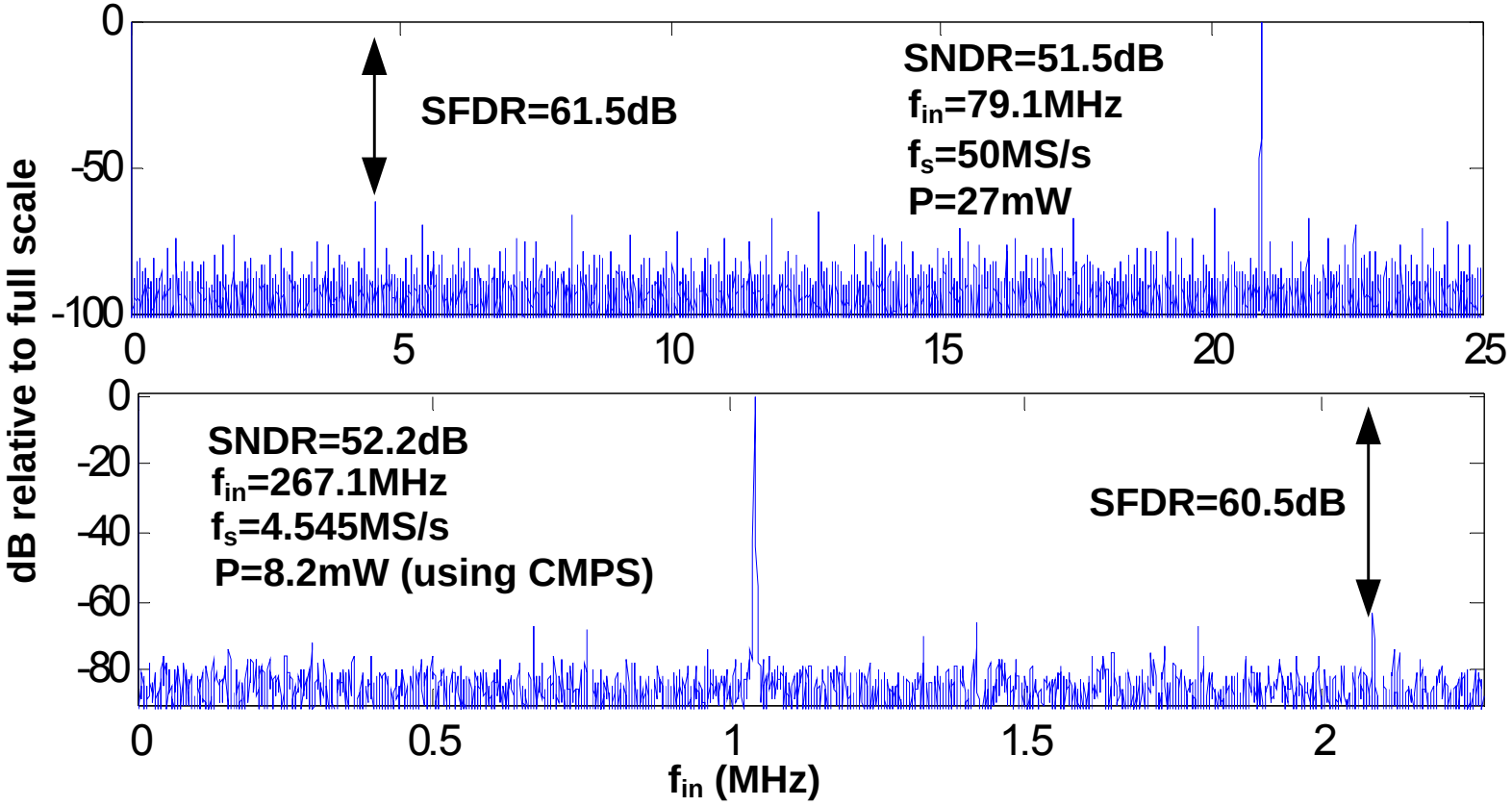


- 1.8V 0.18um CMOS
- Area = 1.21 mm^2

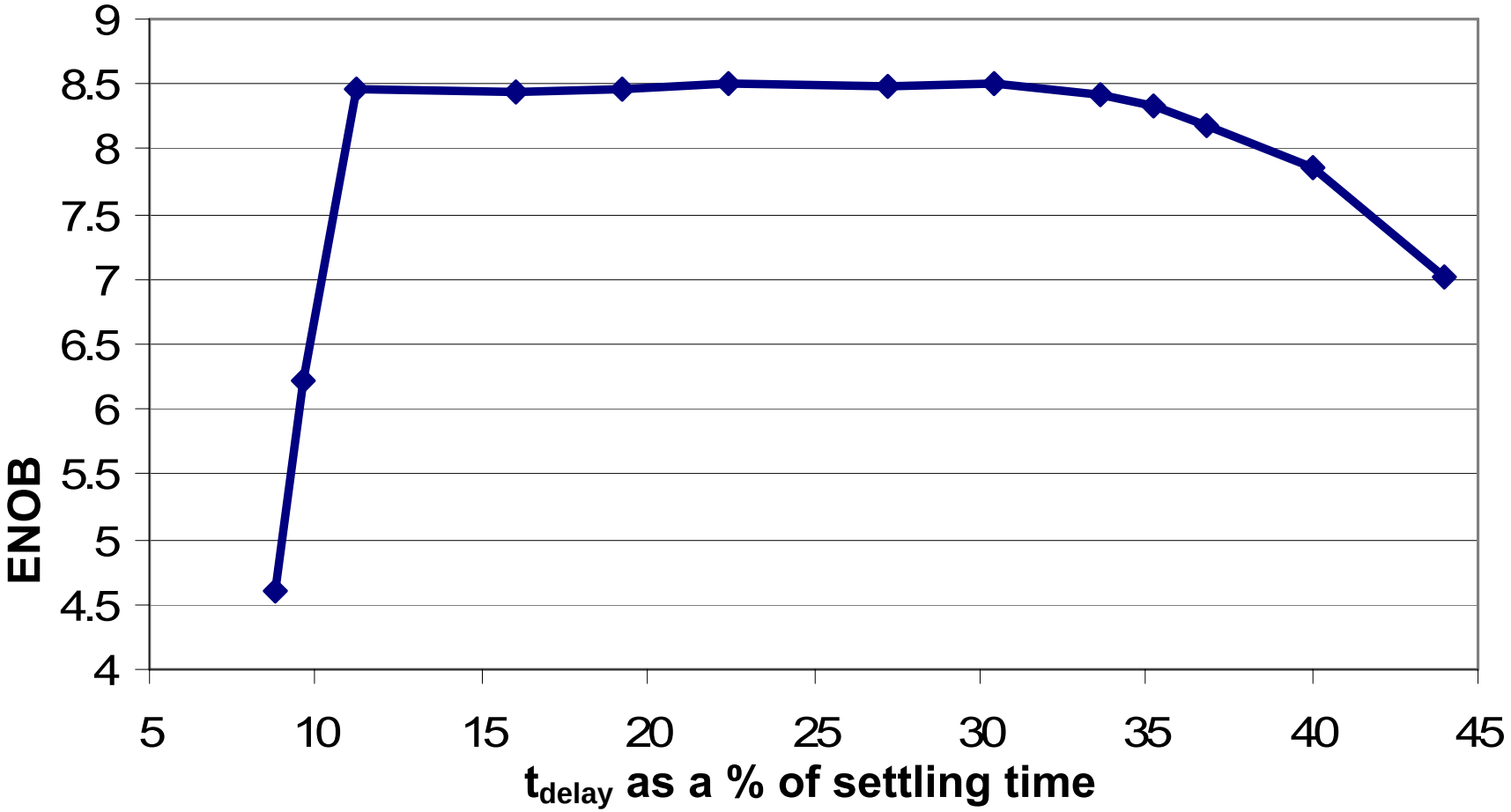
SNDR vs f_{in} (f_s=50MS/s, 4.55MS/s)



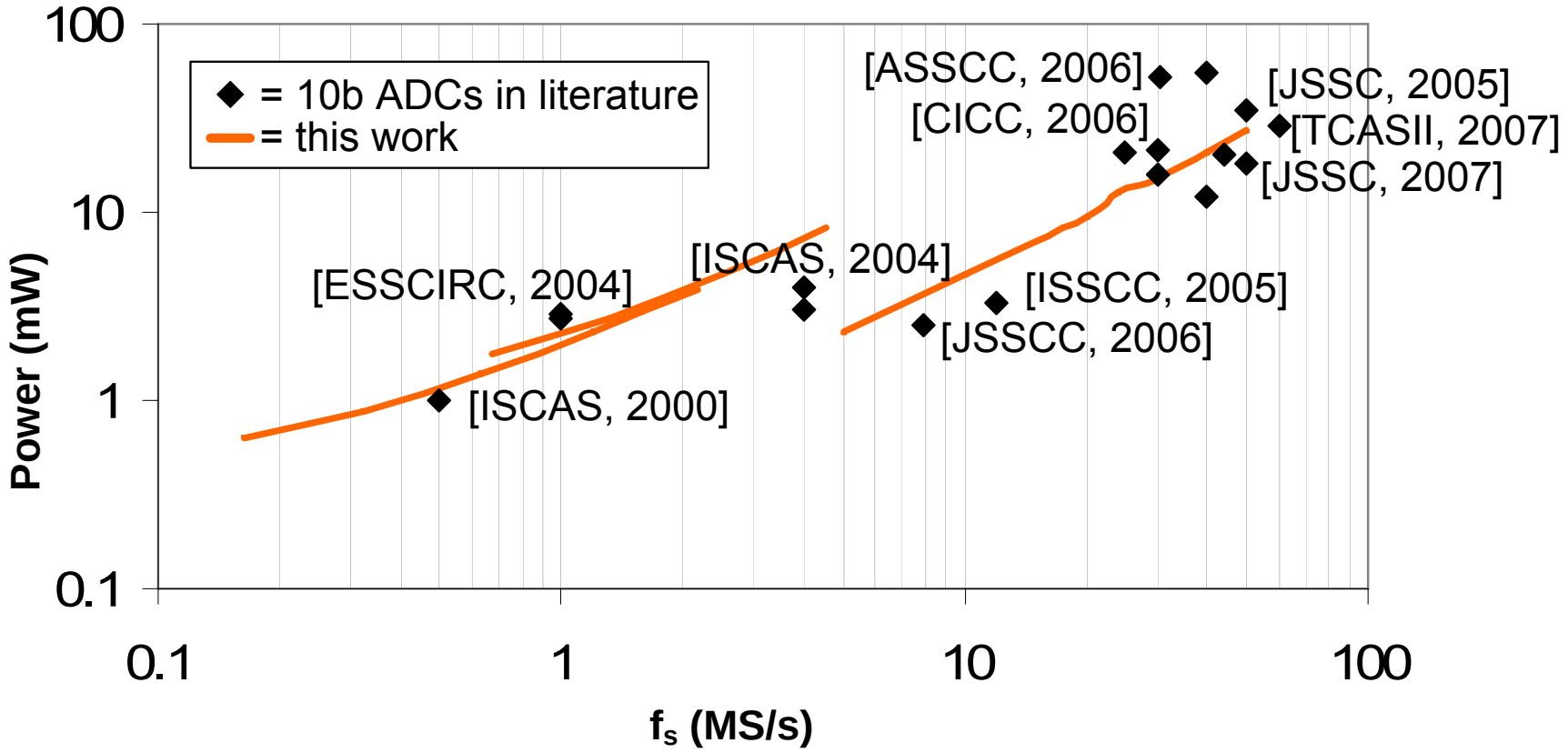
FFT (f_s=50MS/s, 4.55MS/s)



SNDR vs. t_{delay}



Power vs. sampling rate



- At 50MS/s power reduced from 35mW to 27mW compared to [Ahmed, Johns Dec '05 JSSC]
  - >20% reduction in power by removing S/H

Summary

Technology	1.8V 0.18um CMOS
Sampling rates (fs)	<164kS/s - 50MS/s
Power	<0.6mW - 27mW
SNDR	> 51.5dB for all fs
SFDR	> 60.5dB for all fs
input frequency range	0 - 267MHz
Power of [Ahmed, Johns, JSSC, 2005] @ 50MS/s	35mW
Power of this work @ 50MS/s	27mW

Conclusions

- Presented architecture to eliminate front-end S/H that does not rely on matching
  - Power reduction of >20% by using technique of this work
- Method to improve settling behavior of Rapid-Power-On opamps

Acknowledgements

- The generous funding from the National Sciences and Research Council of Canada (NSERC)

- The fabrication services of the Canadian Microelectronic Corporation (CMC)