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Session 9.2

A 50MS/s 9.9mW Pipelined ADC with 58dB SNDR in 0.18µm CMOS Using Capacitive Charge-Pumps

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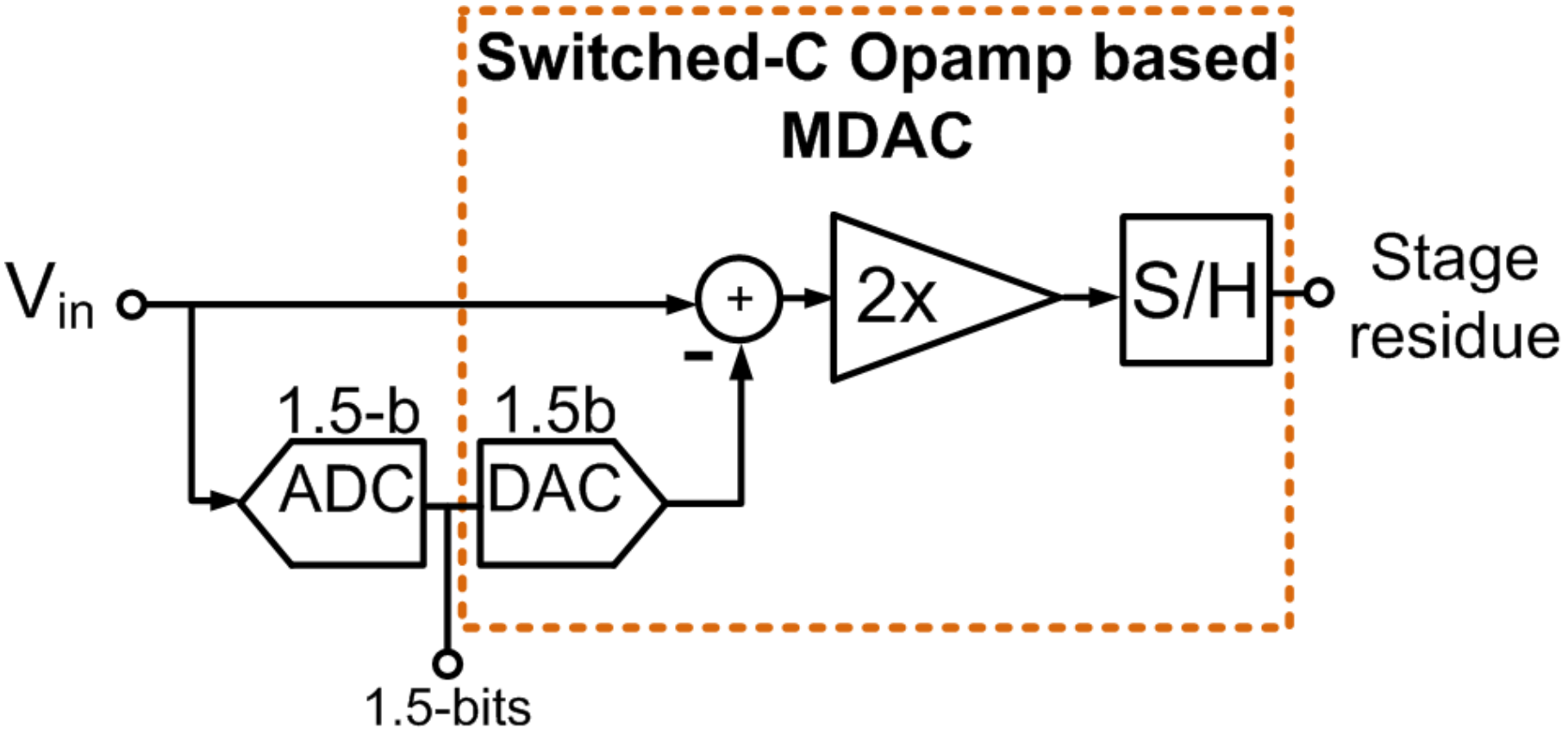
Overview

- Motivations
- State of the art
- Approach of this work
  - Low power capacitive charge-pump based gain
  - Differential stages without CMFB
- Measurement results
- Summary

Motivations

- **Low power:**
  - Increase battery life in mobile applications
  - Enable cheaper packaging in wired applications
- **Simple topology**
- **Trade analog with digital**
  - Scales better with newer technology

Typical 1.5-bit pipelined ADC stage



- Opamp needed for 2x gain → large power consumer
- **Opamp power → gain x bandwidth**

State of the art approaches

- Substitute opamp with more power efficient topologies
  - [Murmann et al, ISSCC '03]
  - [Sepke et al, ISSCC '06]
  - [Hu et al, VLSI '08]

- Limitations of prior approaches:
  - Complex topology (e.g. non-linear calibration), or
  - Single-ended/Psuedo-differential, or
  - Linearity below 8-bits

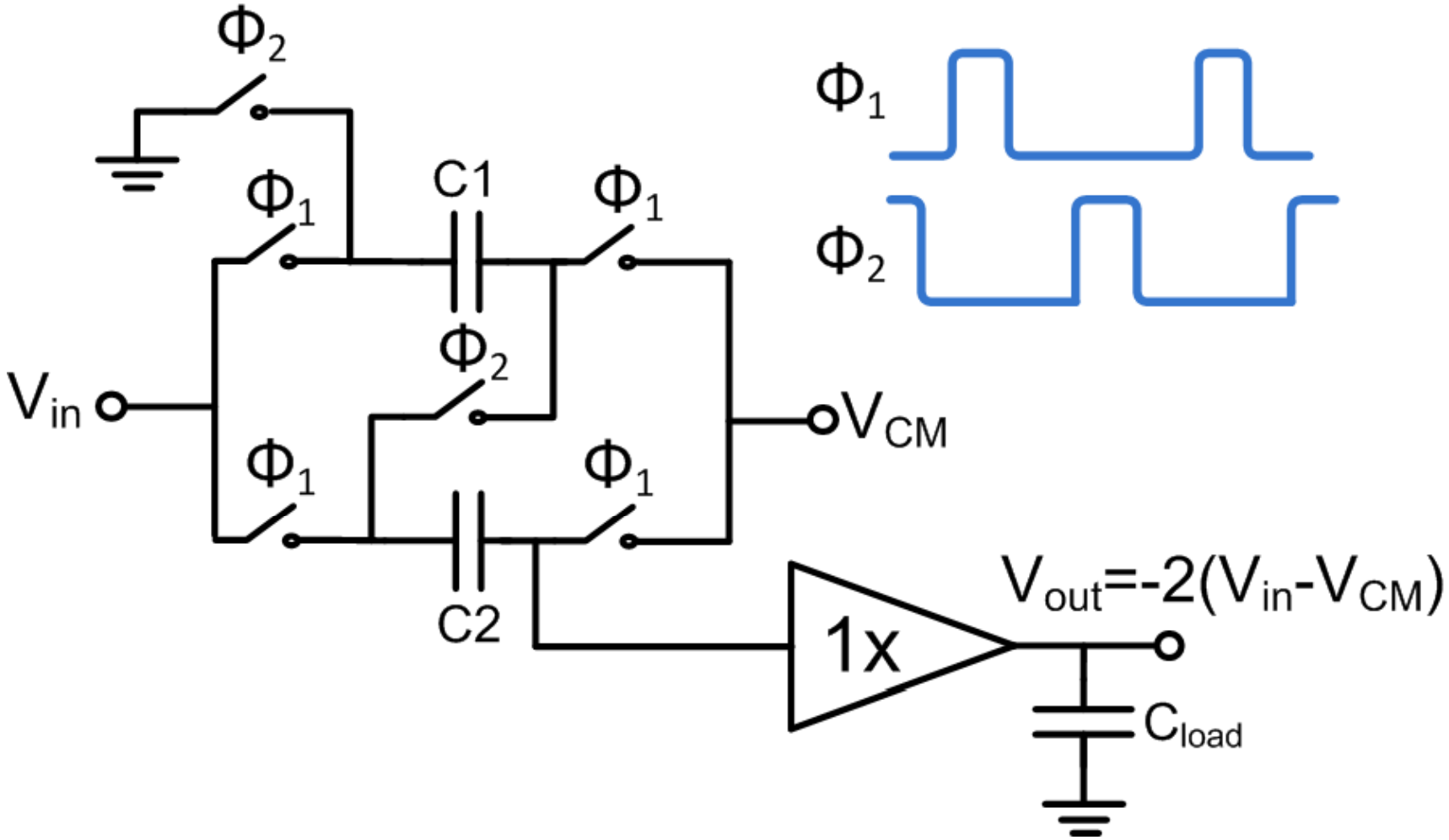
Goal of this work

- Low-power, opamp-free topology that:

  1. A simple topology and digital calibration scheme
  2. Has a differential topology
  3. Can achieve a linearity > 10-bits

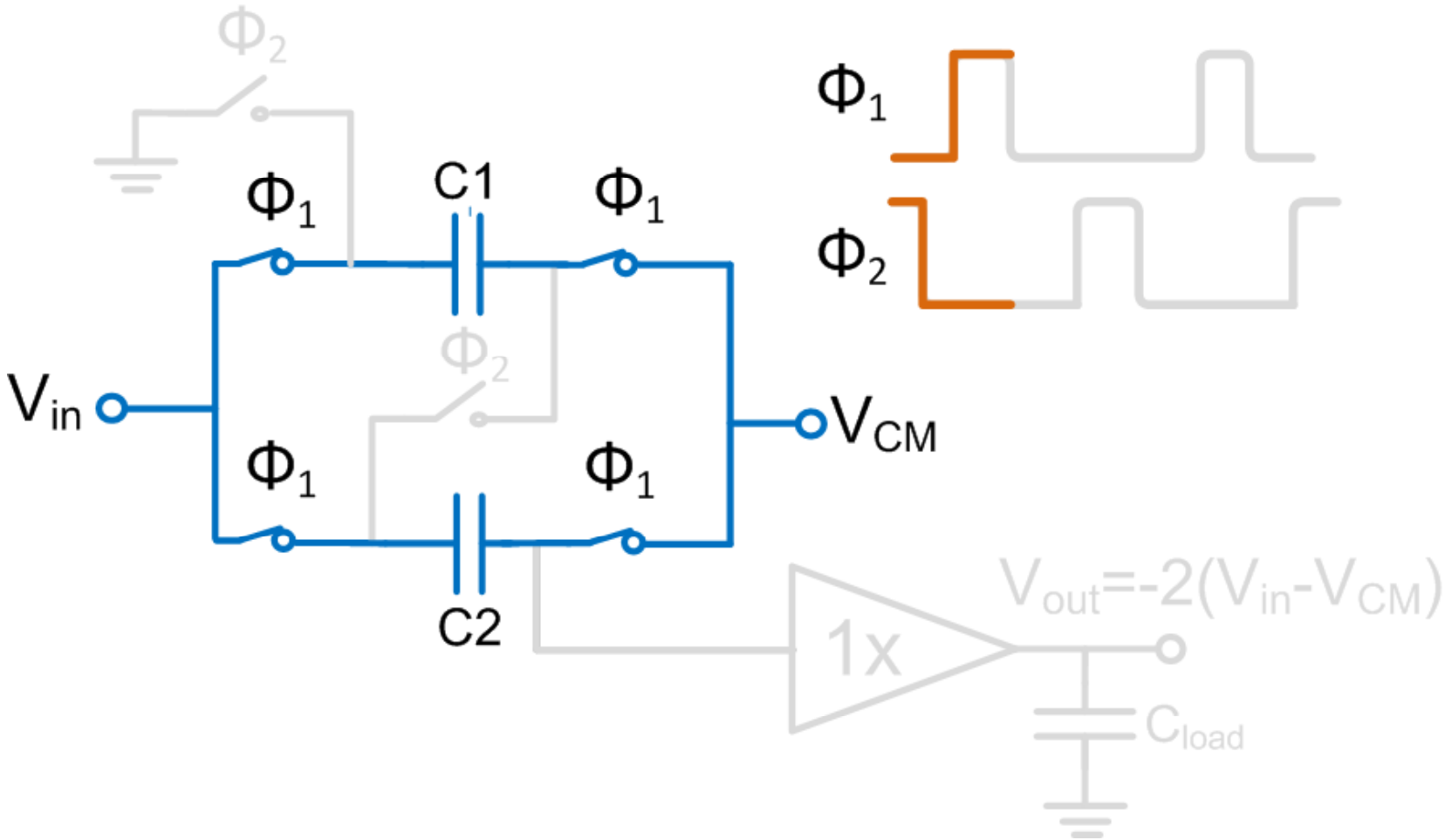
- Proof-of-concept Pipelined ADC → 10-bit / 50MS/s
  - Variety of applications from digital communication to medical imaging

2x gain using charge pump



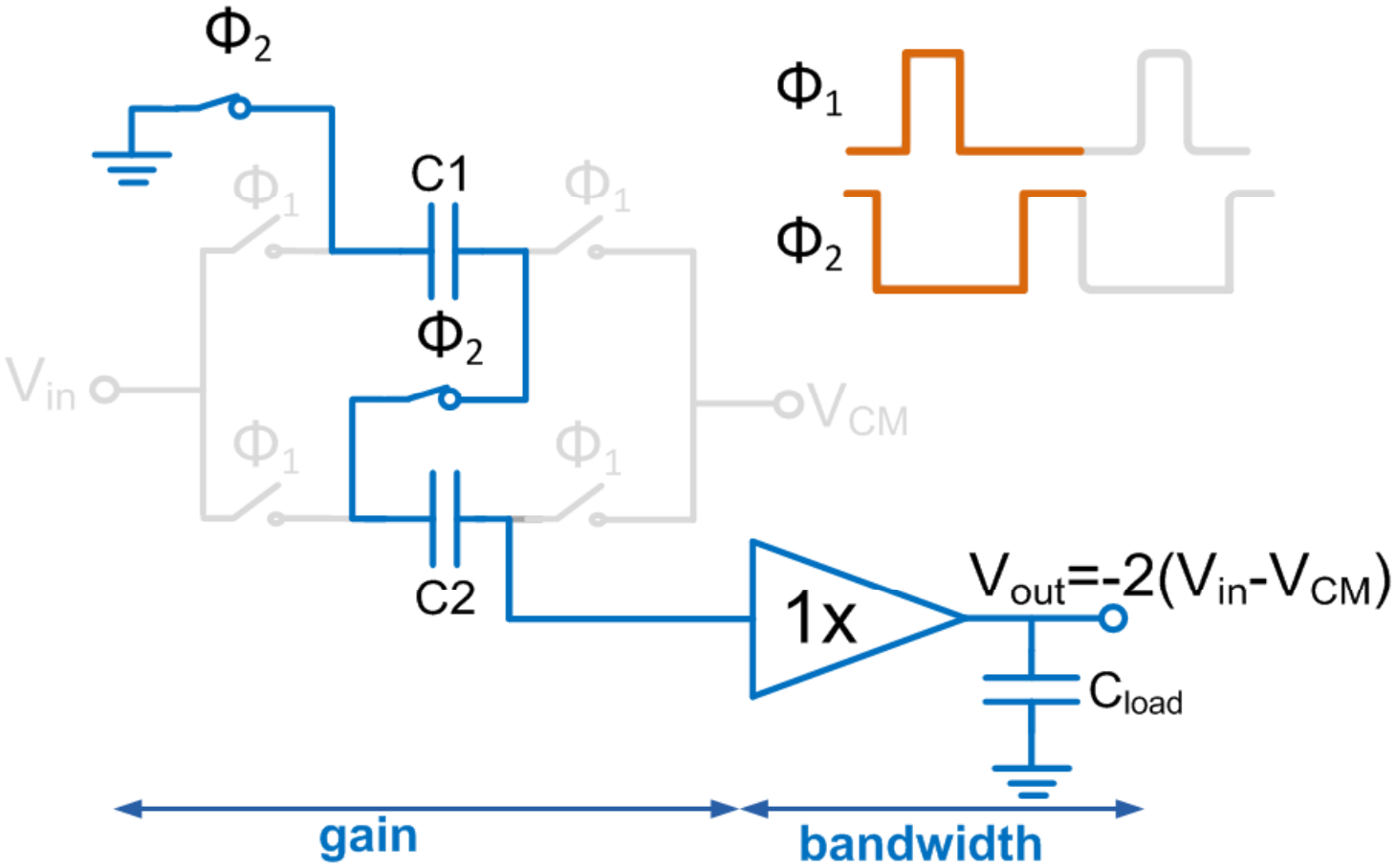
- Capacitive voltage-doubler based approach for gain

during Φ_1



- Input sampled onto two capacitors in first clock phase
- C1=C2

during Φ_2

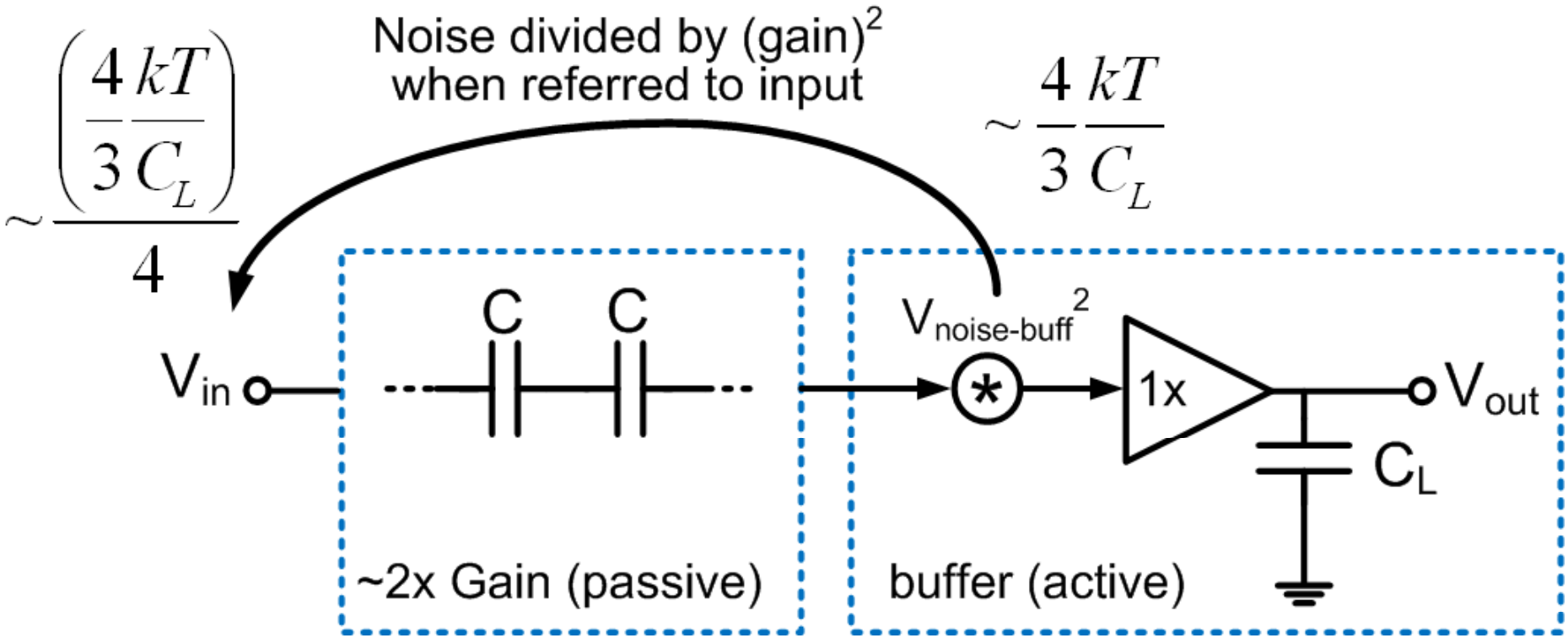


- Gain achieved by charge addition

✓ Low power → **gain-bandwidth tradeoff decoupled**

x CM error also doubled

Reduced active noise

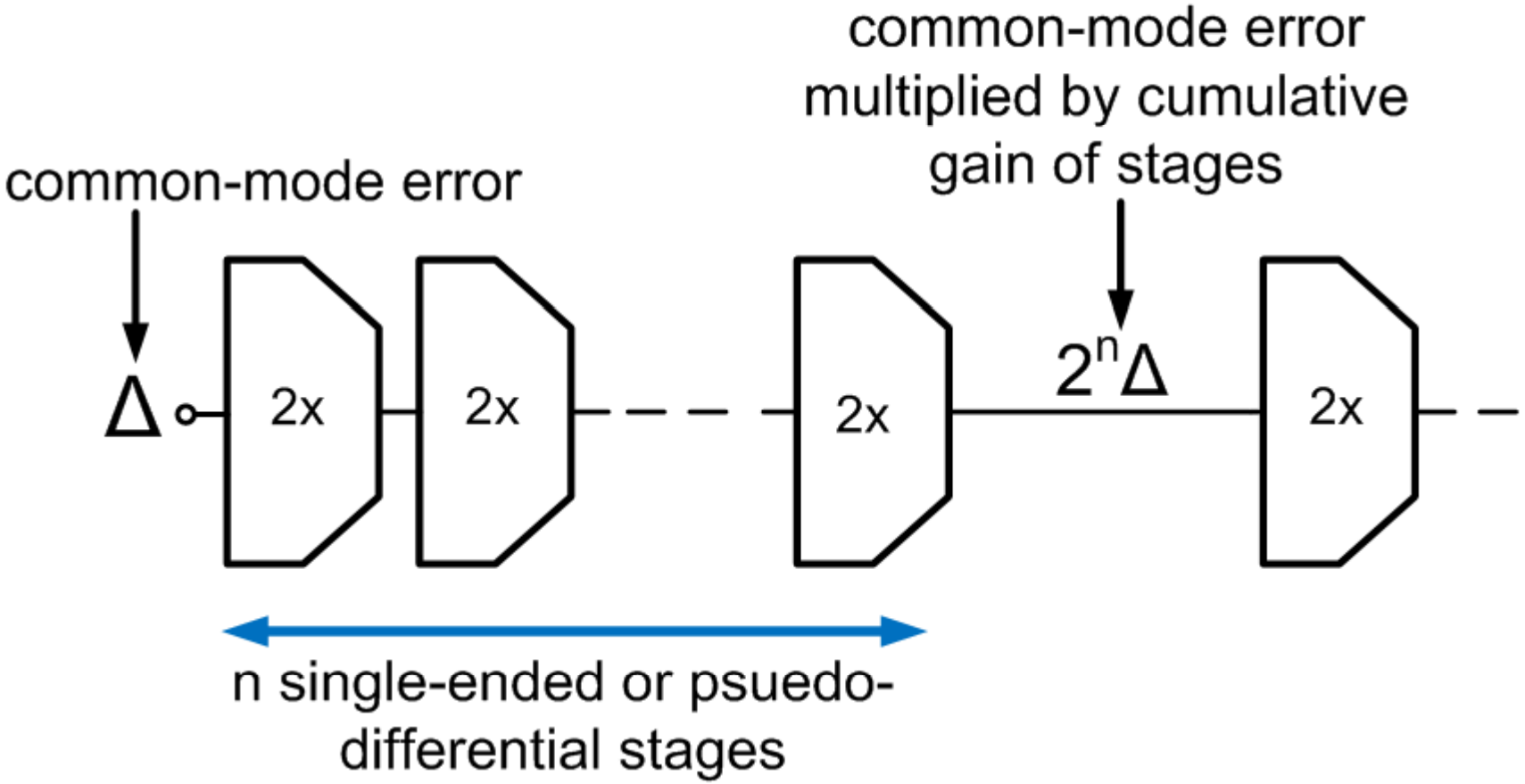


- Small buffer noise → small capacitors → low power
- Cf. → in SC opamp based circuit, opamp noise directly refers to input

Architectural challenges

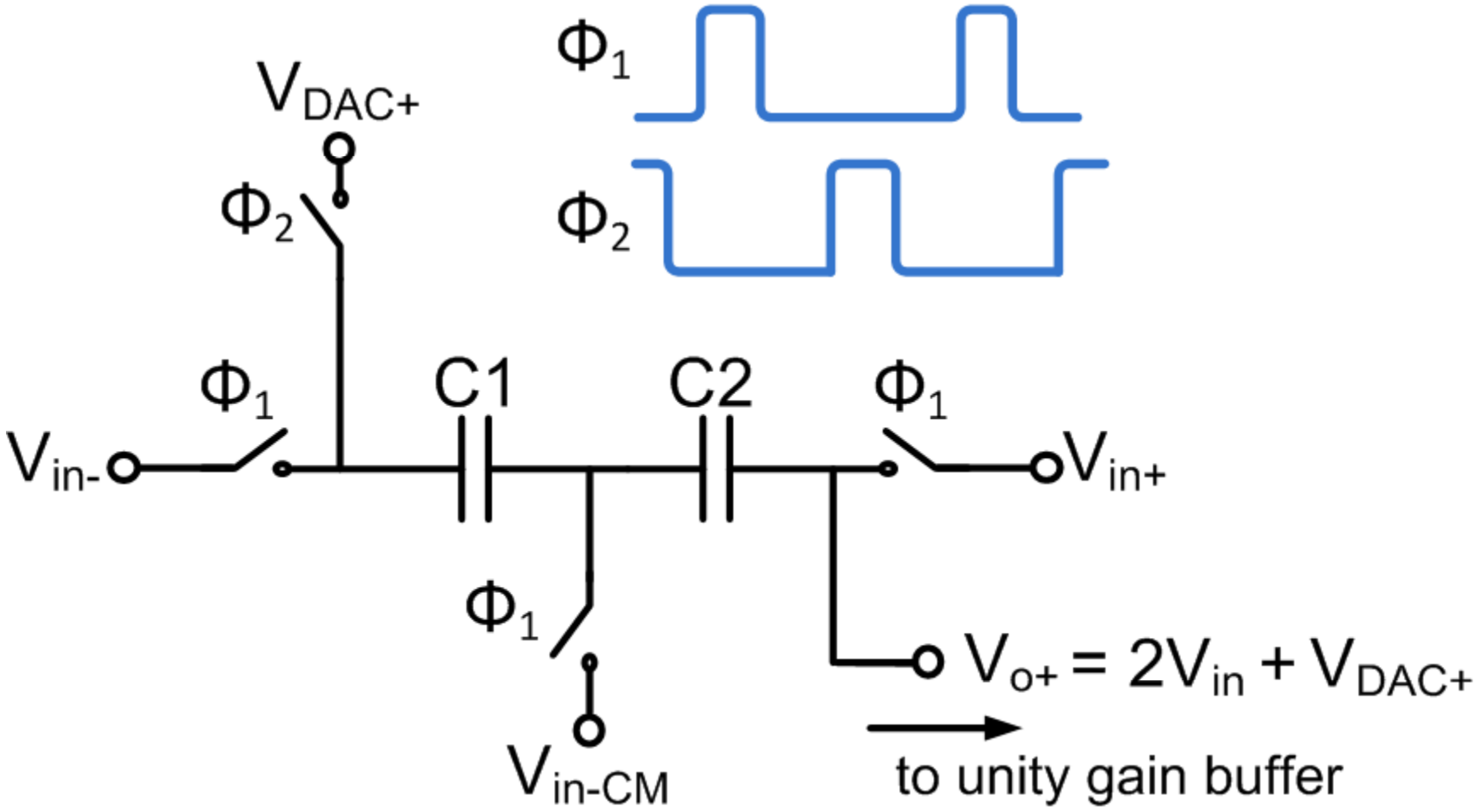
1. How to avoid amplifying common-mode errors
2. Impact of parasitic capacitors
3. Topology of unity gain buffer

Impact of common-mode errors



- Small CM offset at input can saturate backend stages
- Need differential pipeline stages

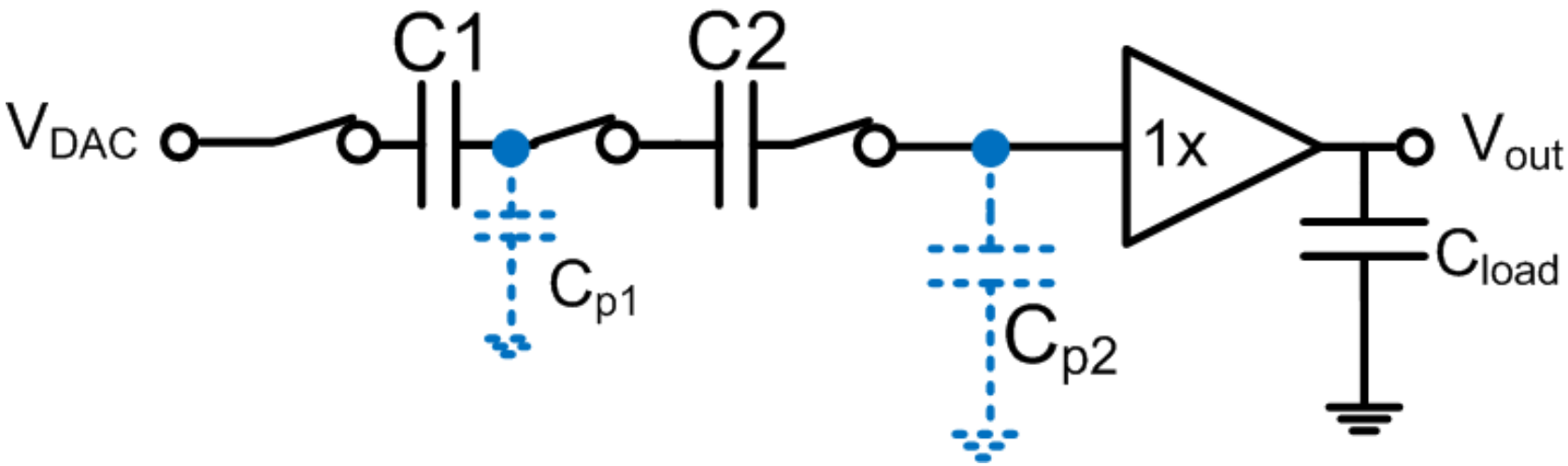
Differential MDAC (+'ve half)



- Input sampled differentially, no need for CMFB
- V_{o+} common-mode set by common-mode of V_{DAC+}

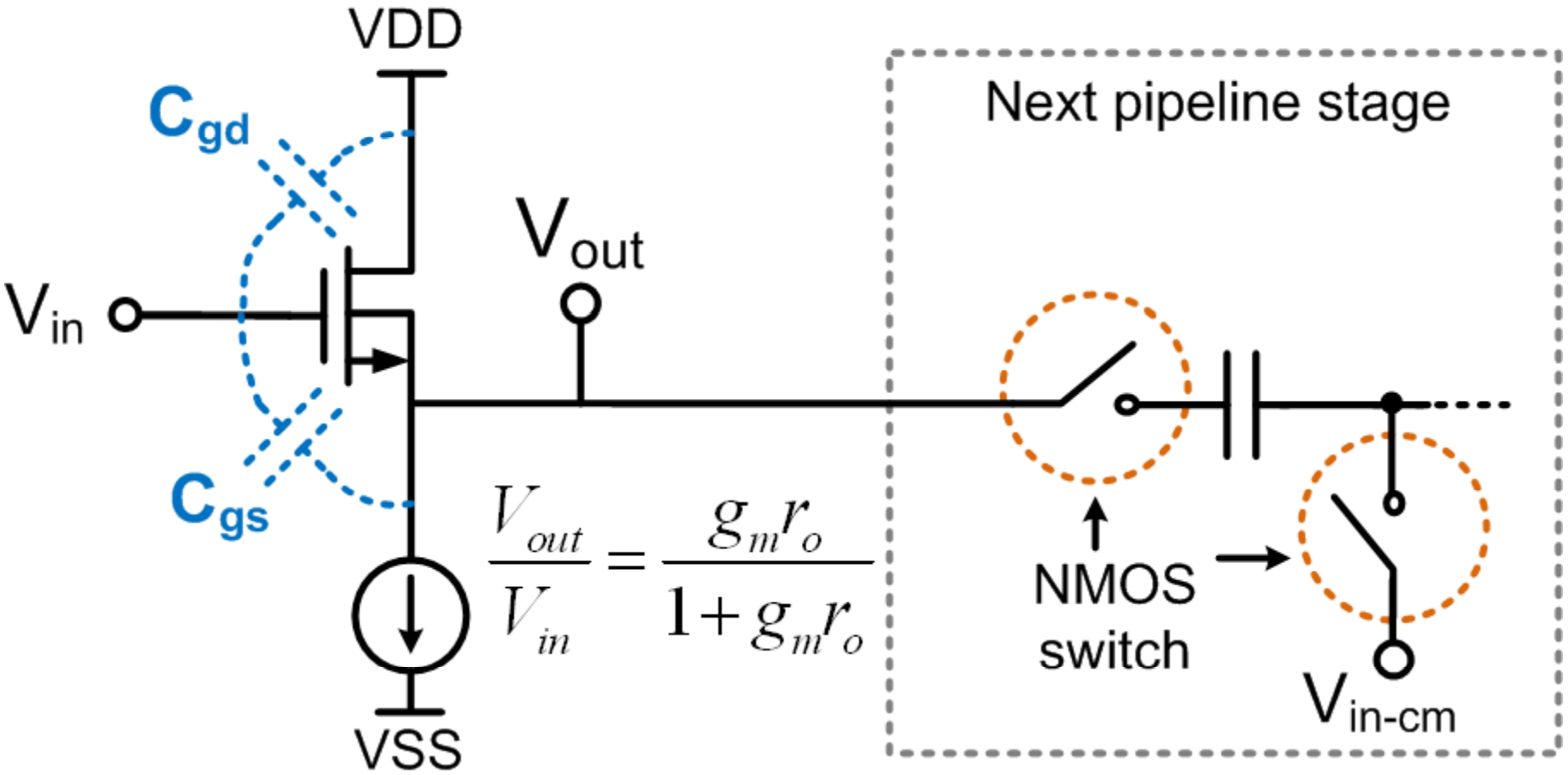
Impact of parasitics on gain

$$V_{out} = -\frac{C1 + C2}{C2 + C_{p2}} V_{in} + \frac{C1}{C2 + C_{p2}} V_{DAC}$$



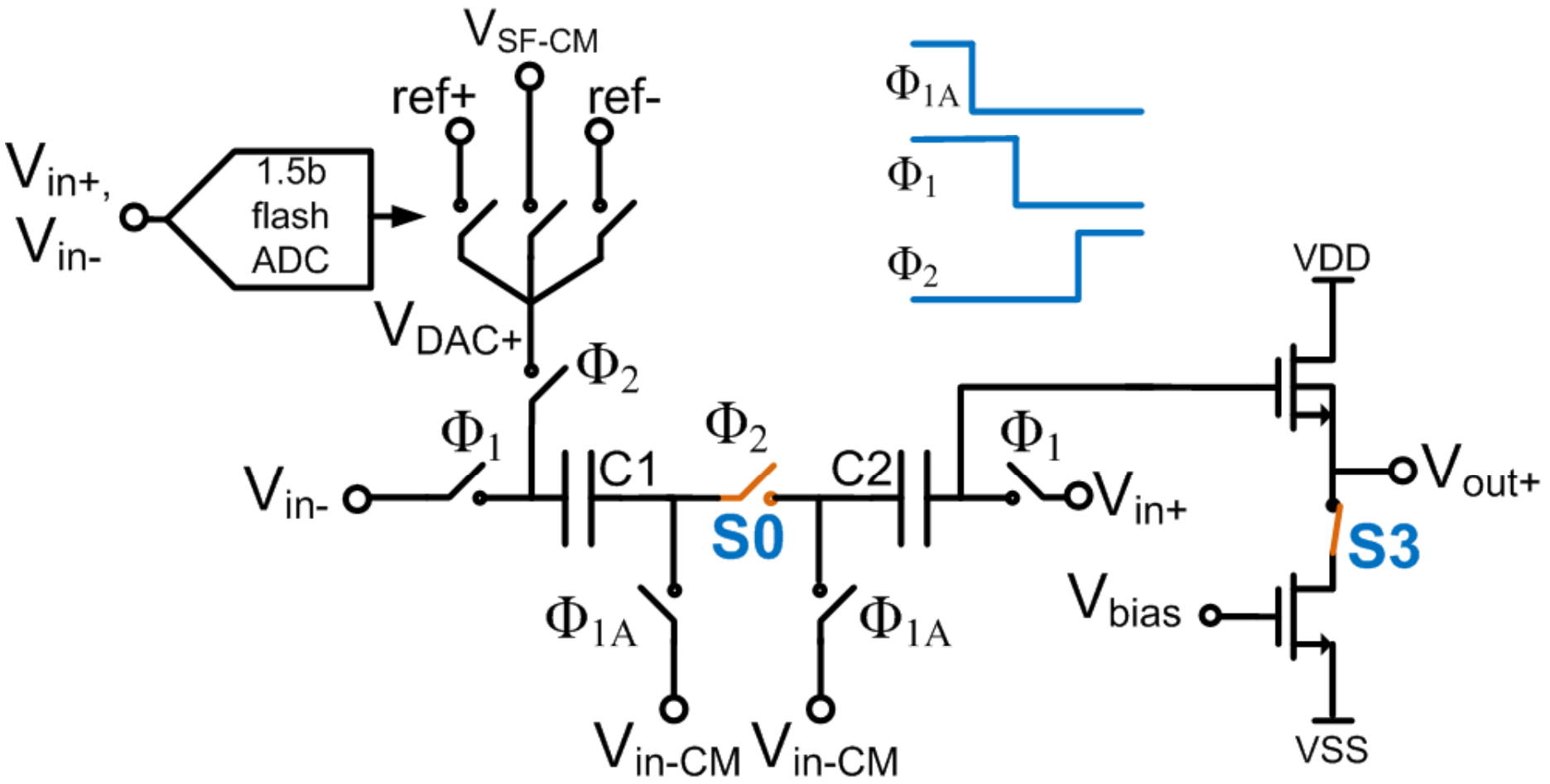
- Linear gain error corrected with digital calibration
- Small switches minimize non-linear parasitics

Unity gain buffer – Source Follower



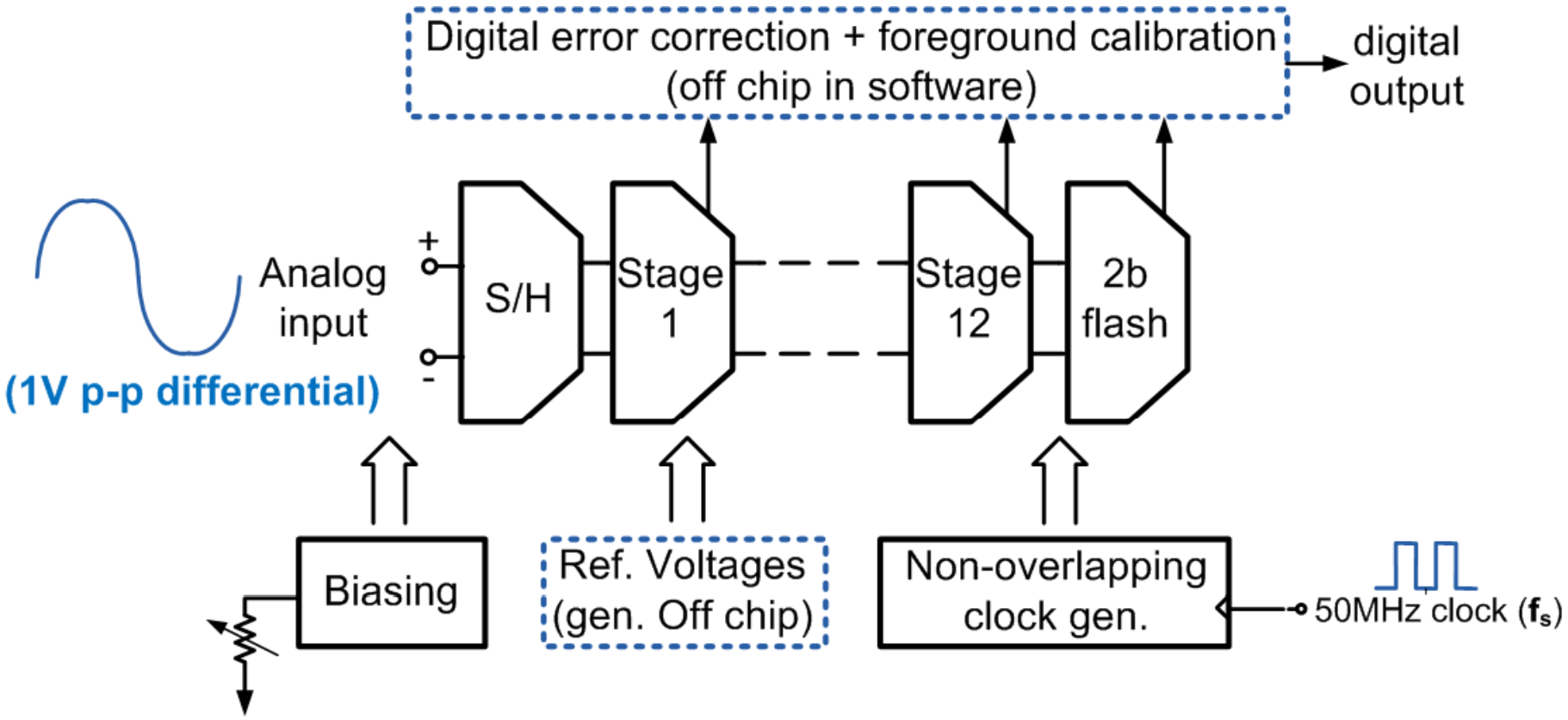
- NMOS S.F. has high g_m, low output common-mode
- small input capacitance → ~C_{gd}

Complete 1.5-b stage (+'ve half)



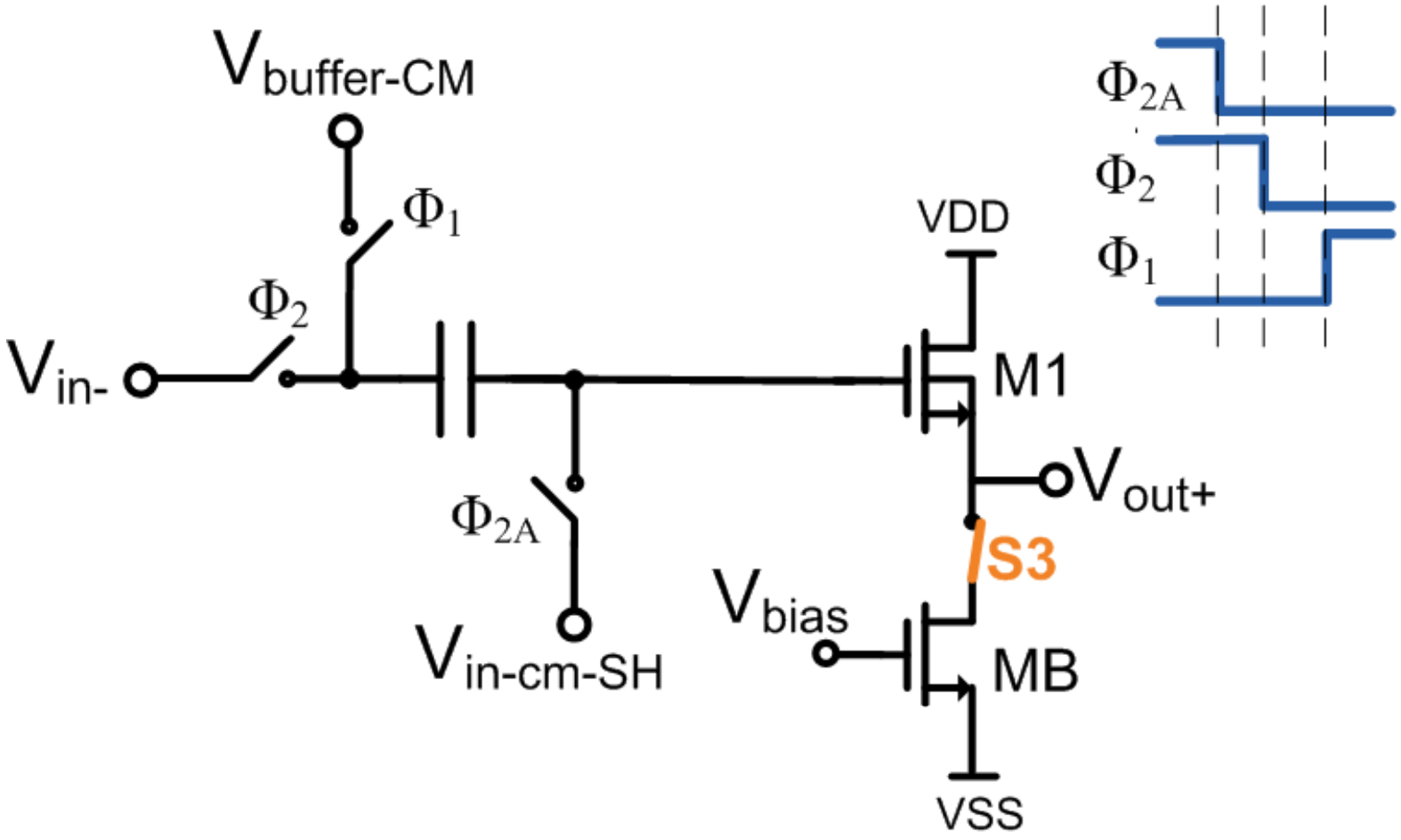
- S0 → ensures bottom-plate sampling→ good linearity
- S3 → to power-off S.F. for half the clock cycle

Pipelined Topology



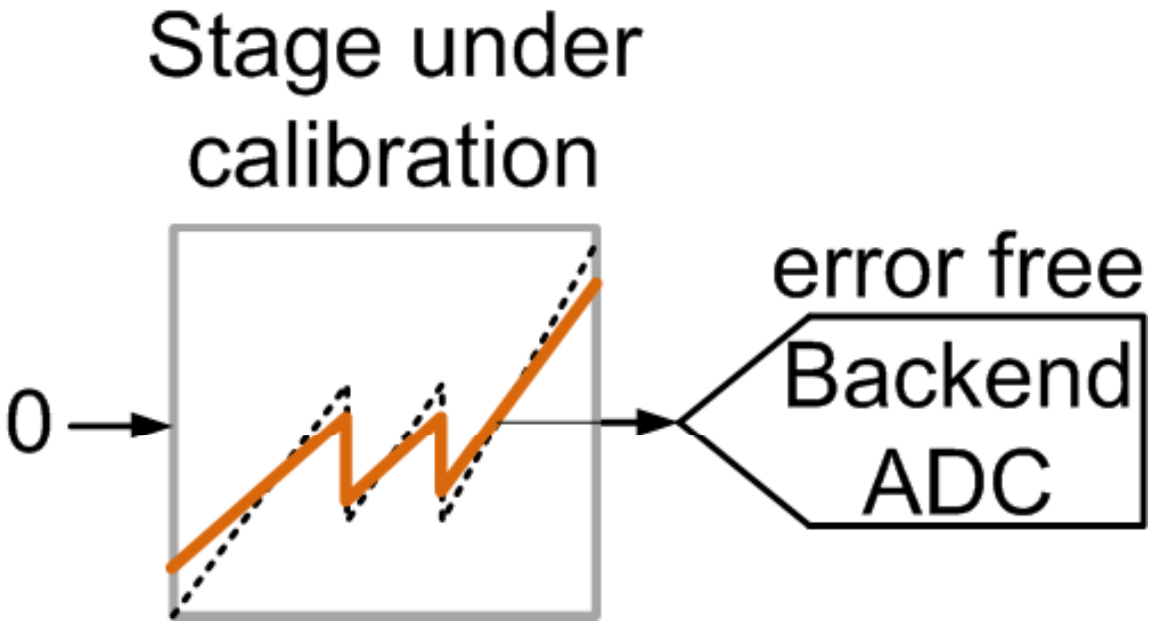
- Stage gain ~ 1.75x → need 12 stages for 10-bits

Front-end S/H (half circuit)



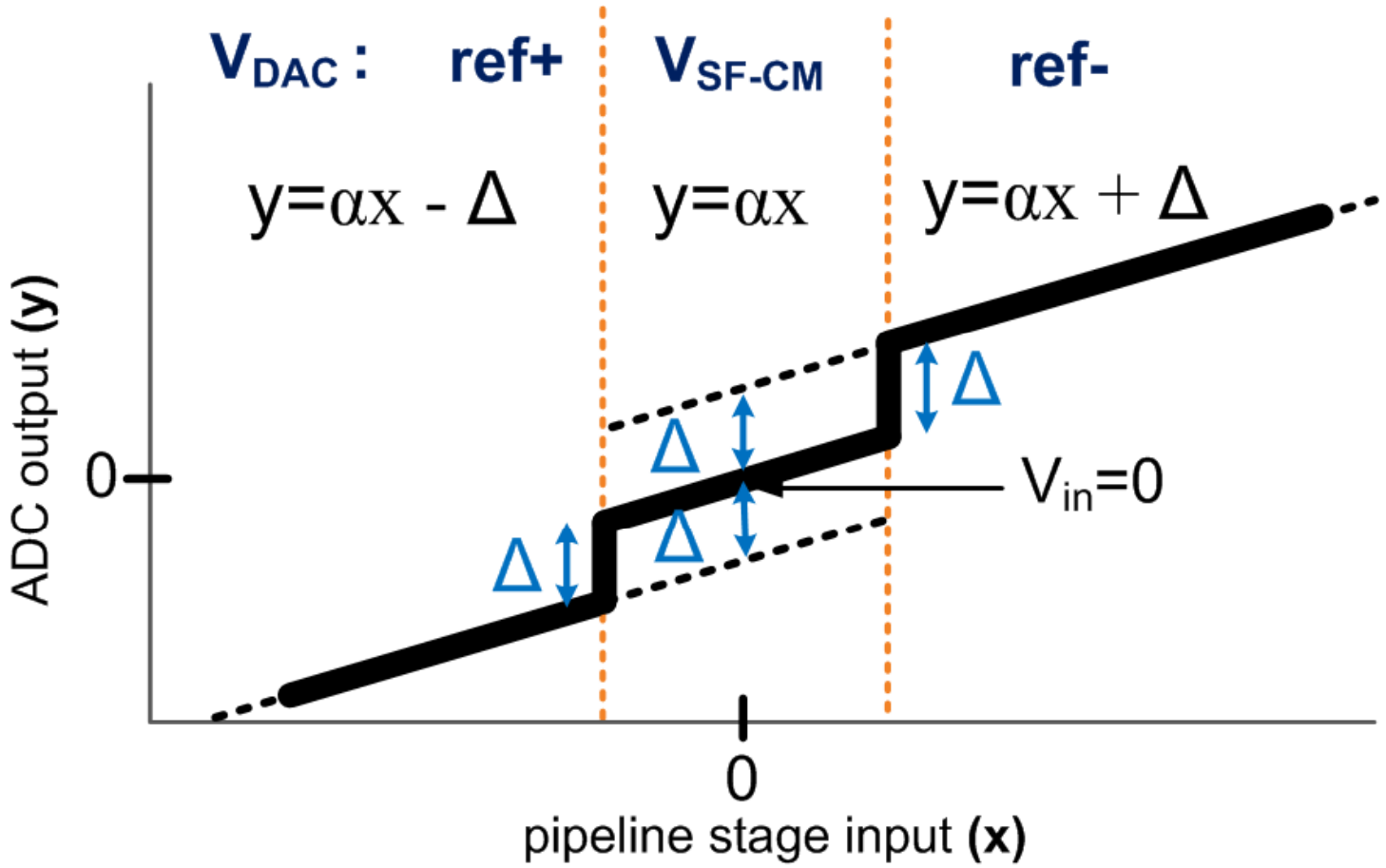
- Low-power, simple approach
- Offset of S/H removed by sampler of next stage

Gain error foreground calibration



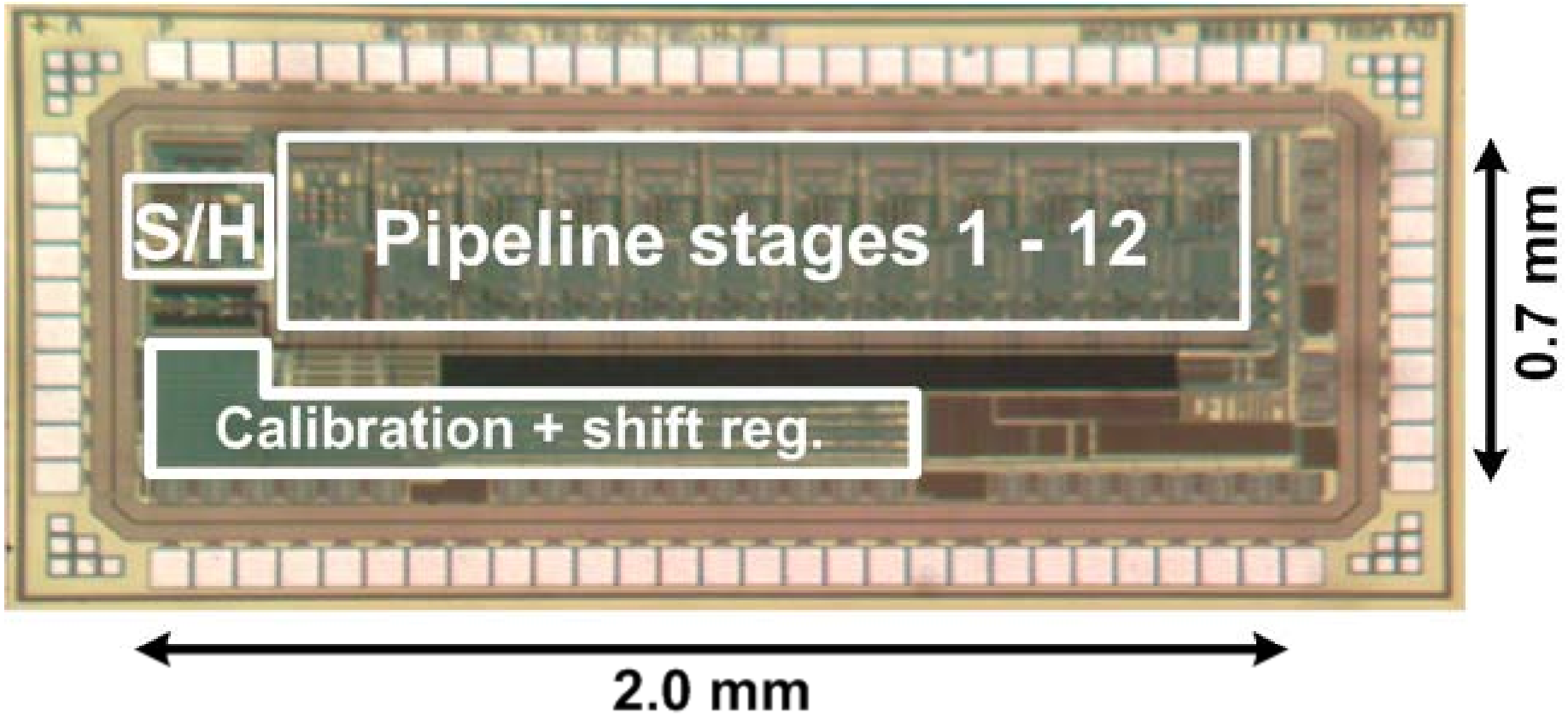
- assume backend ADC error free

Measurement of gain error



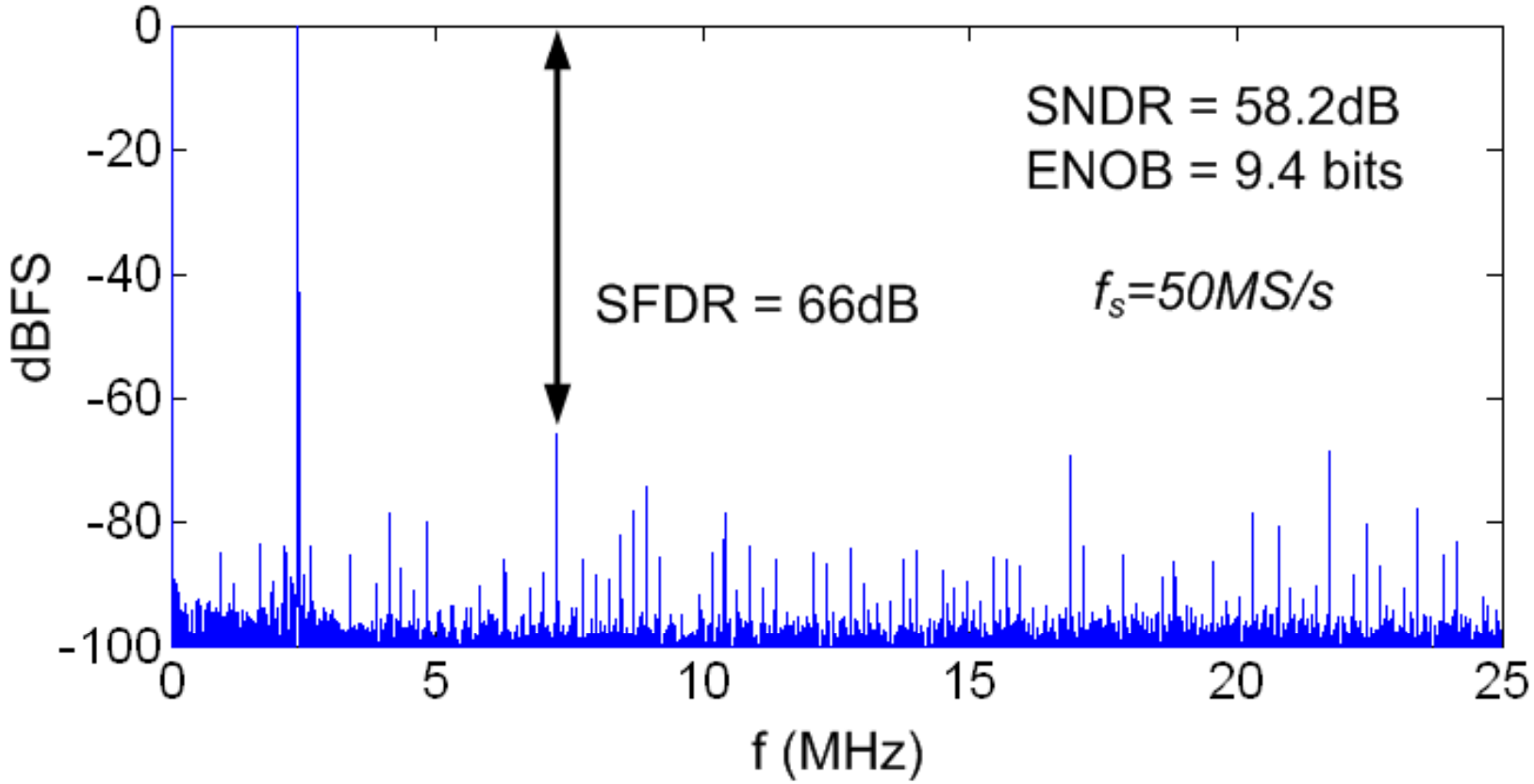
- Set V_{in}=0, toggle DAC voltage to measure Δ
- Recursively calibrate from last stage to first

Chip micrograph



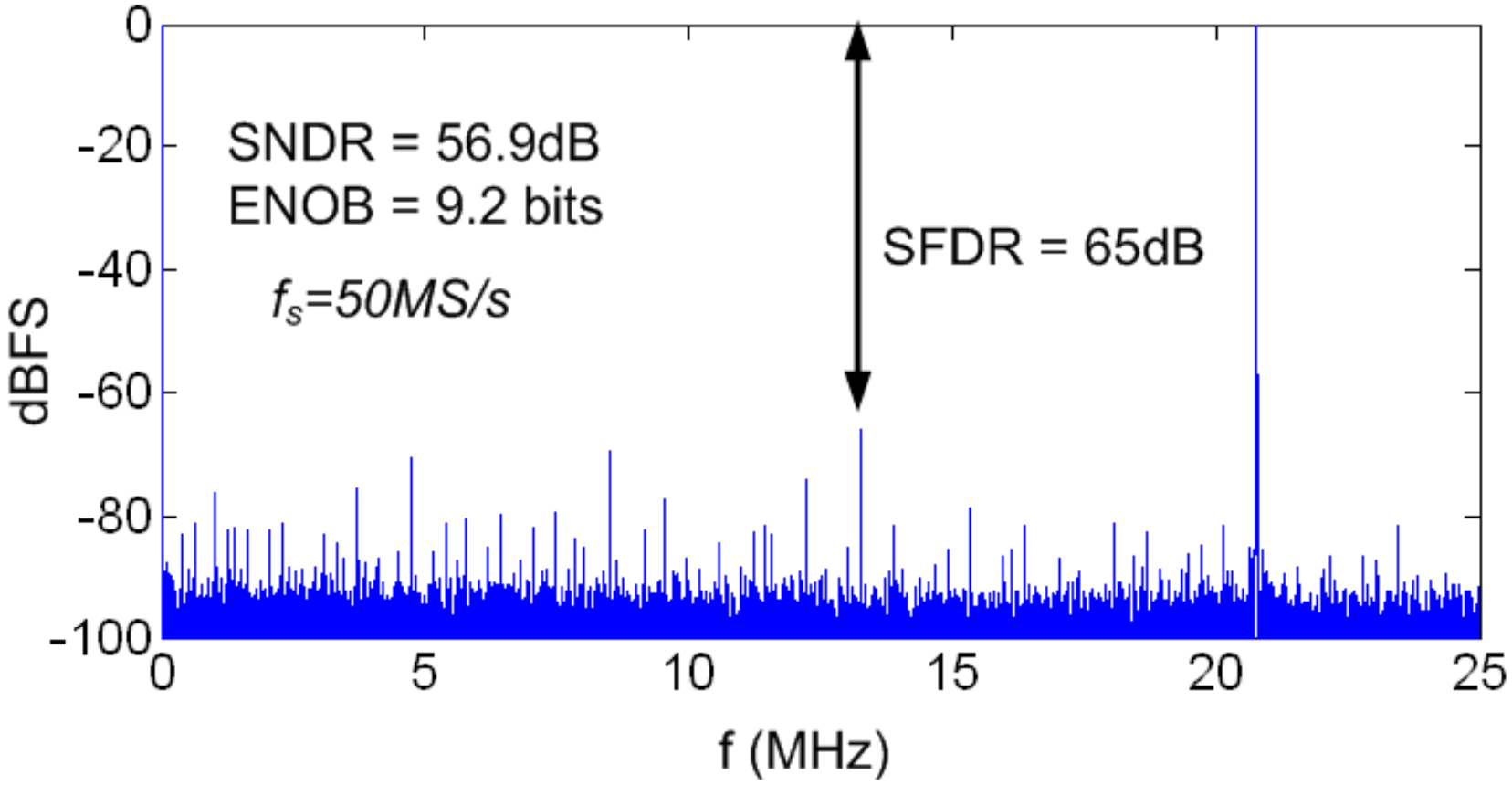
- 1.8V, 0.18µm CMOS process
- 1.4 mm^2 → includes test circuitry, decoupling caps.

32,768 pt FFT (f_{in}=2.4 MHz)



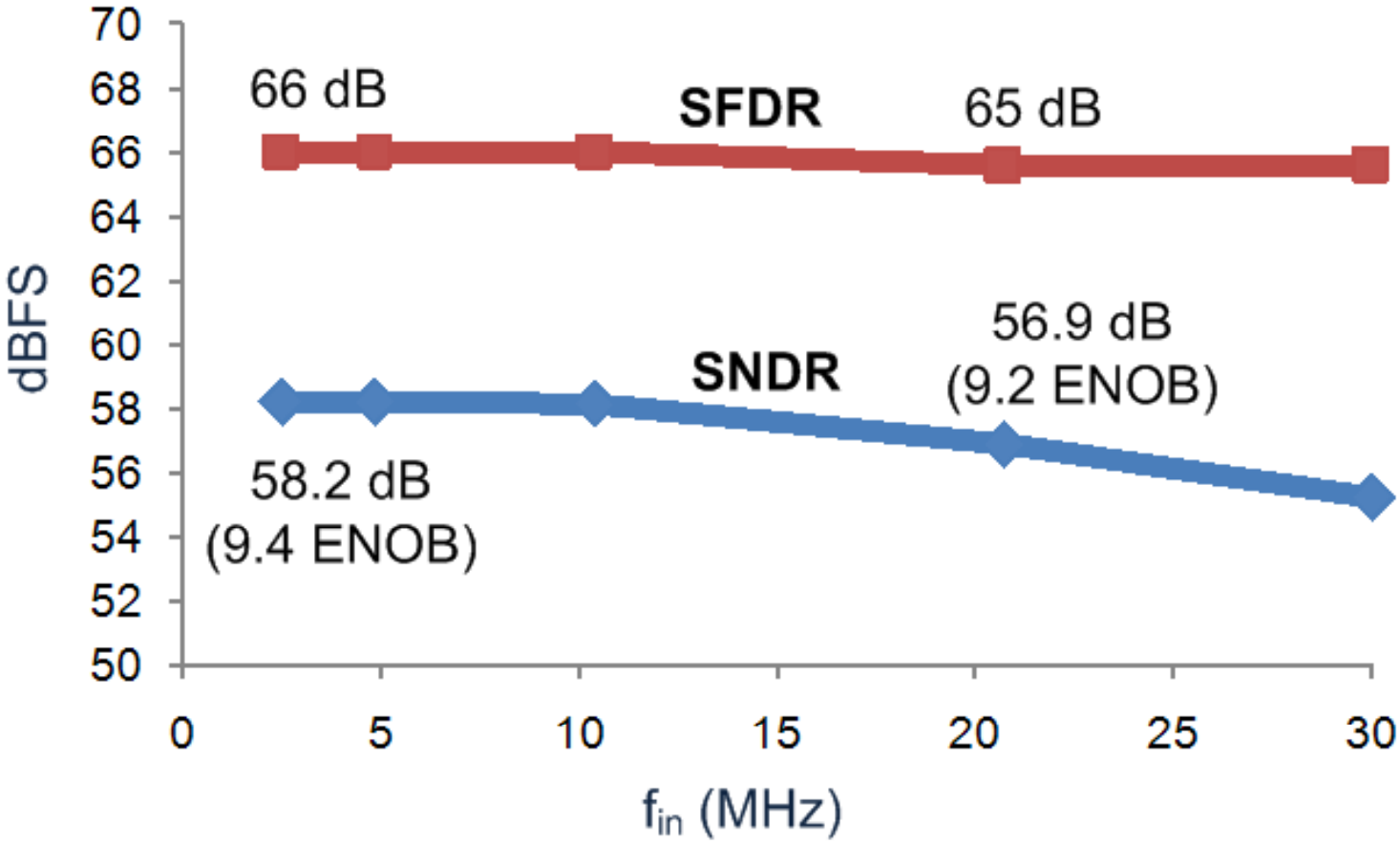
- Even order distortion strongly suppressed

32,768 pt FFT (f_{in}=20.7 MHz)



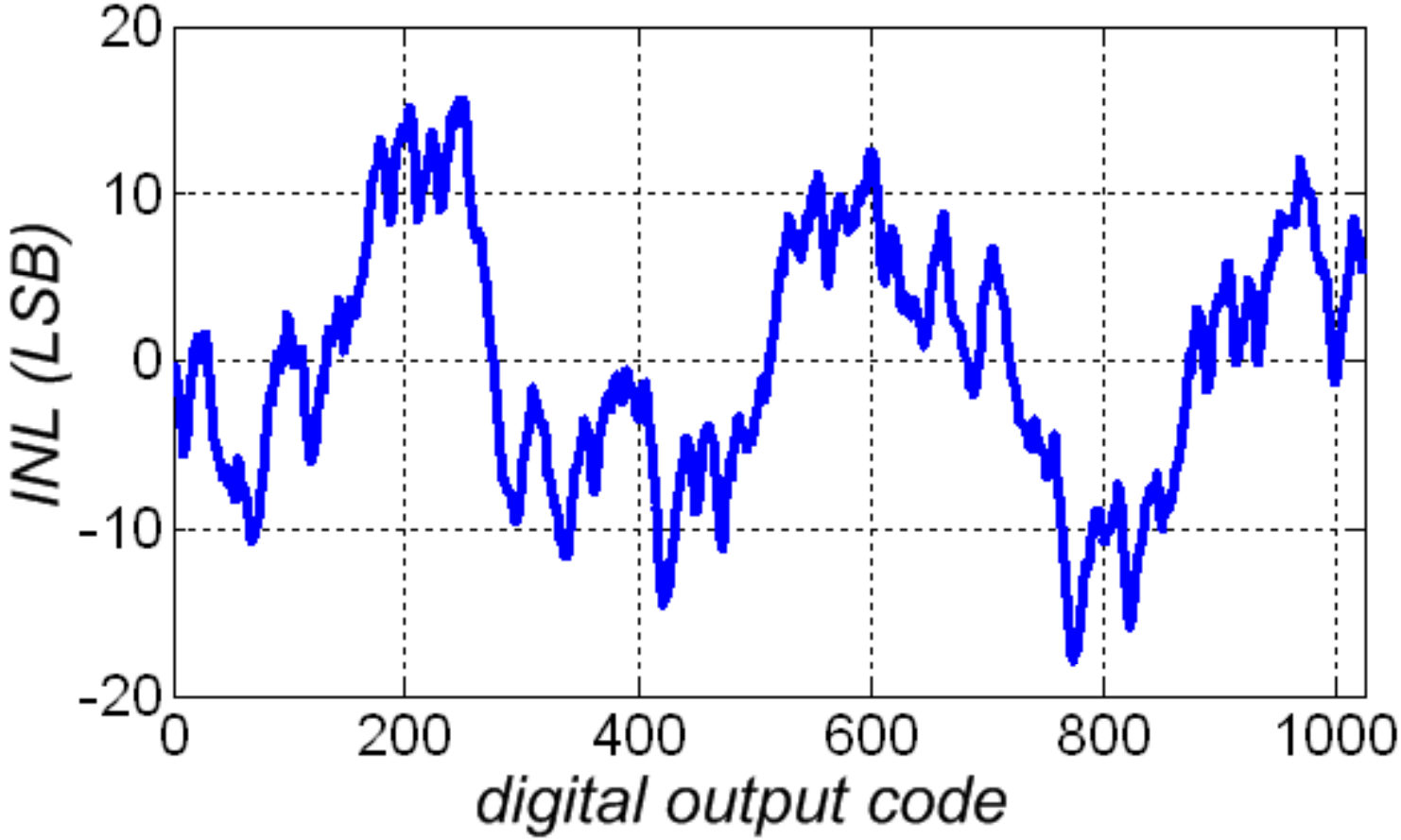
- > 9-bit ENOB for Nyquist bandwidth

f_s=50MS/s, SNDR/SFDR vs. f_{in}



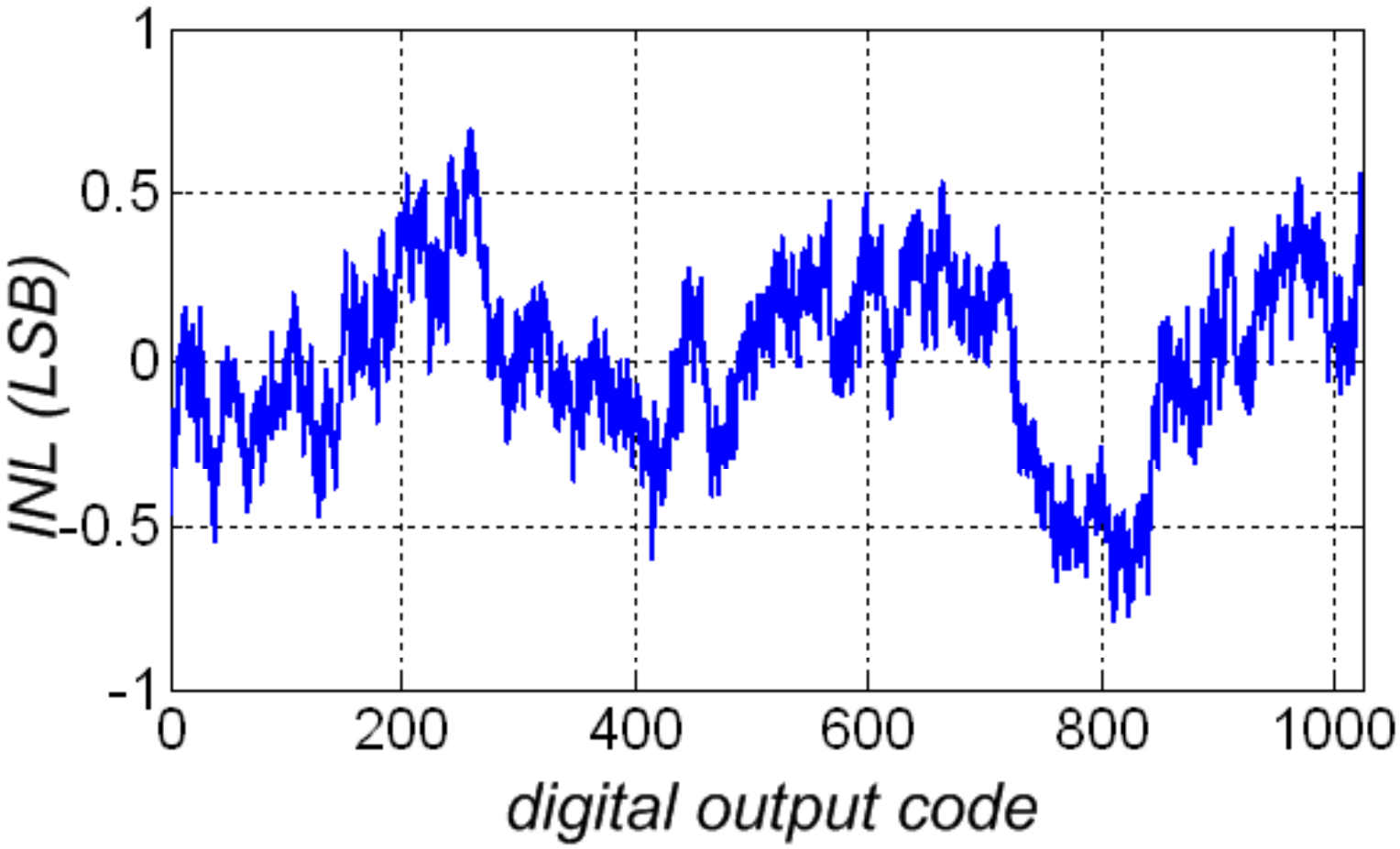
- **Power: 3.9mW (active) + 6mW (clocking) = 9.9mW**
- Ref. voltages (not included) → 0.34mA

INL (before calibration)



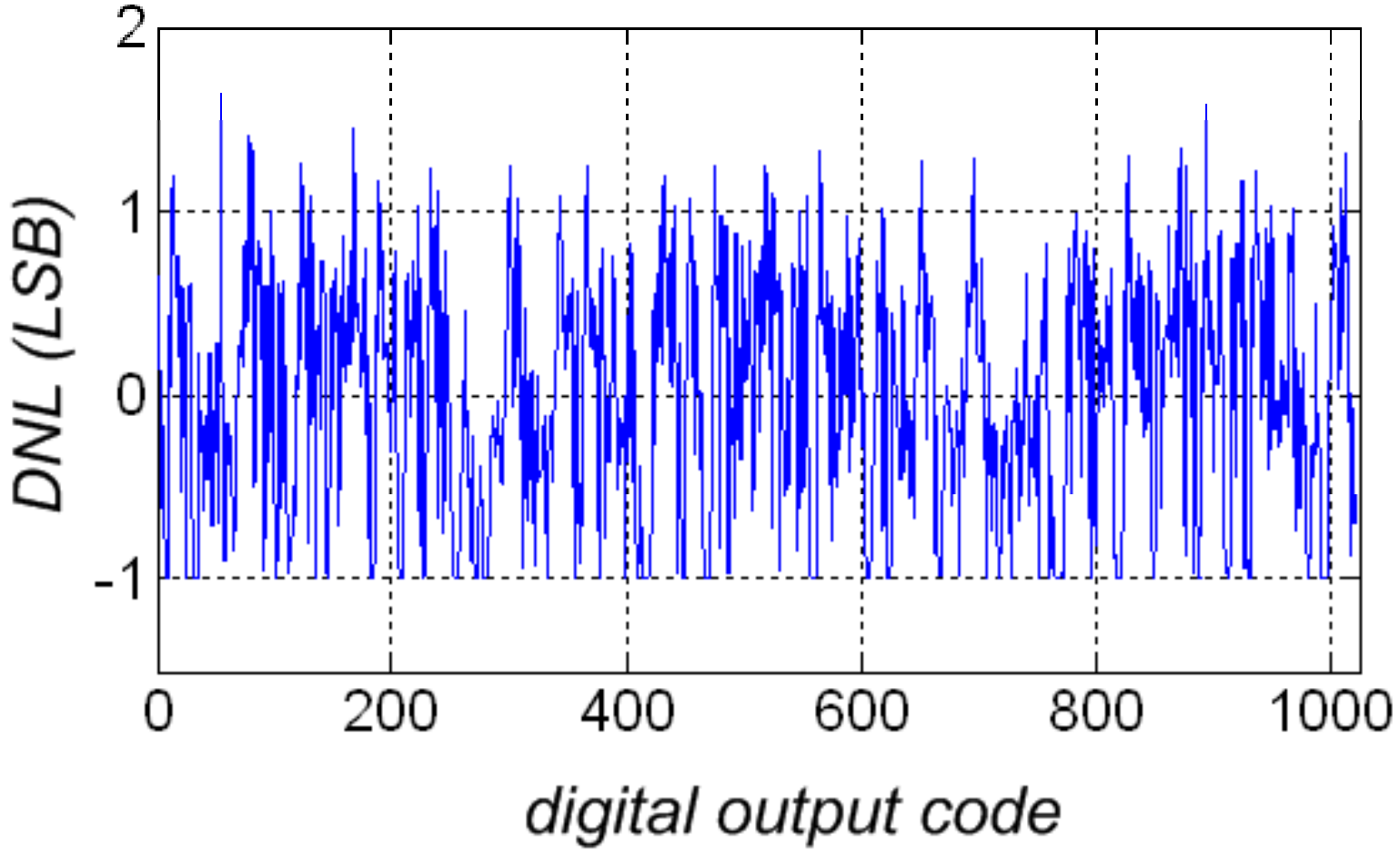
- Peak INL = +15.7/-17.9 LSB (LSB @ 10-b level)

INL (after calibration)



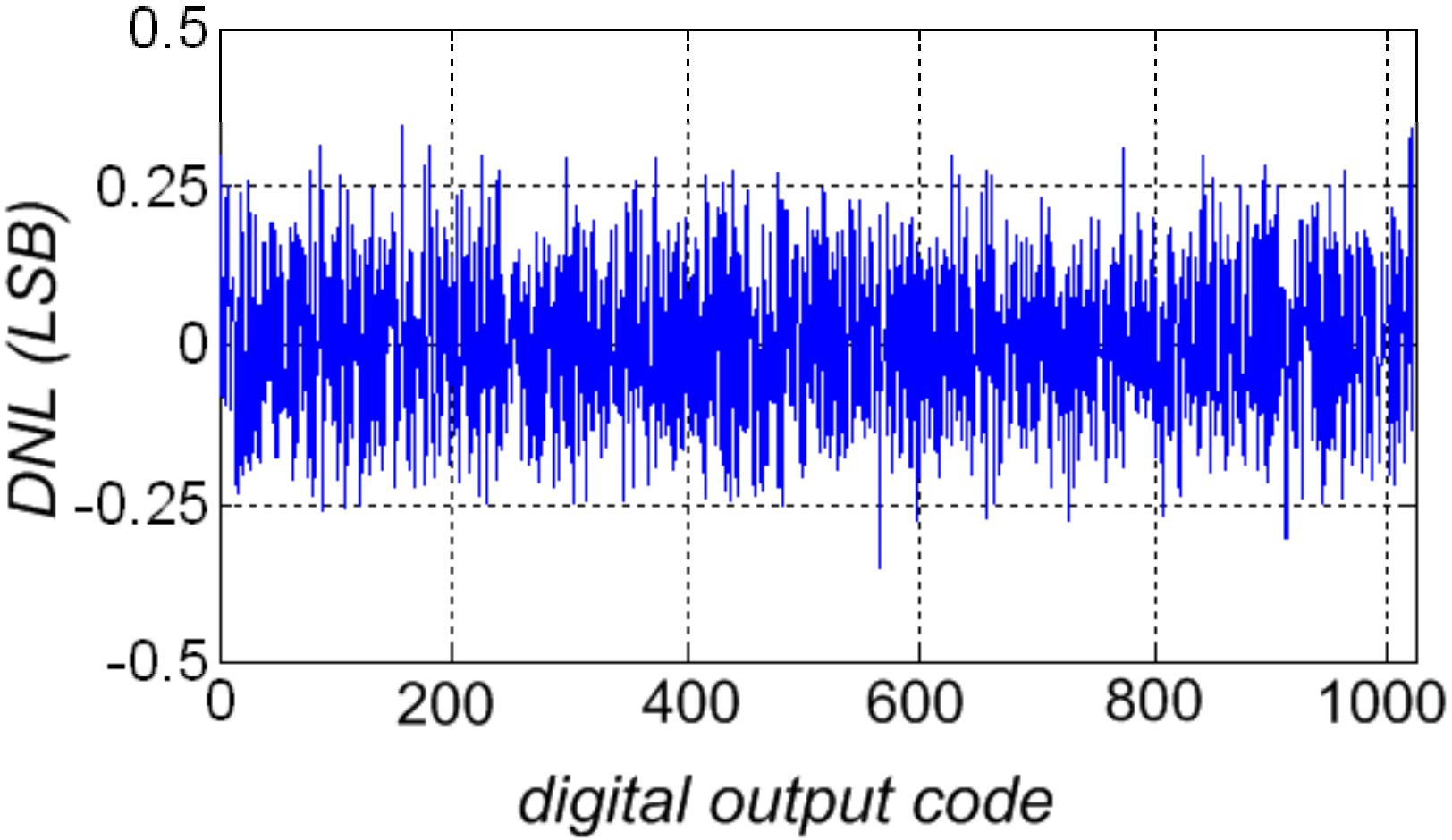
- Peak INL = **+0.7/-0.8 LSB**

DNL (before calibration)



- Peak DNL = **+1.6/-1 LSB**

DNL (after calibration)



- Peak DNL = **+0.35/-0.35 LSB**

Calibration robustness

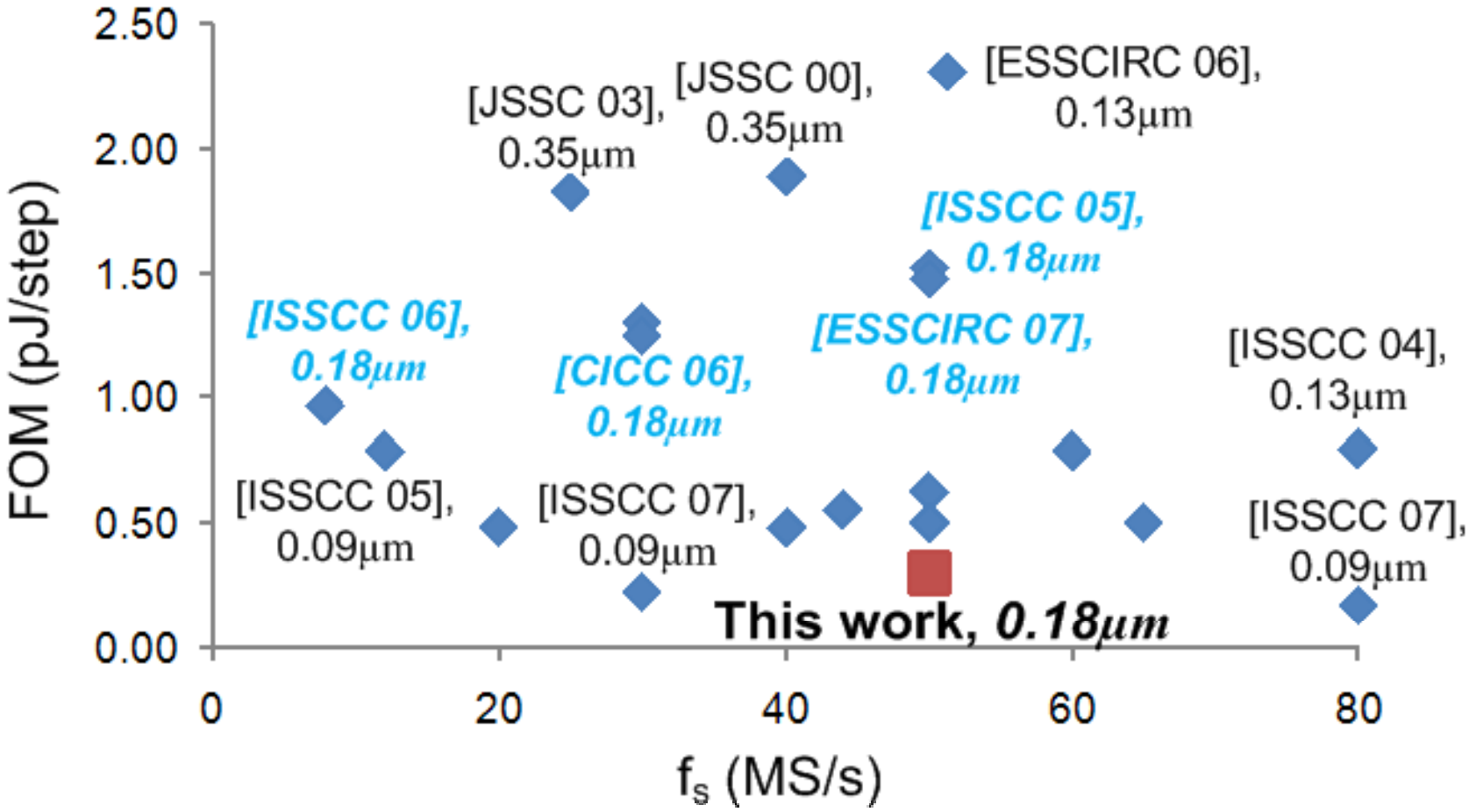
- Calibration coefficients fixed, ADC output measured while varying:
  - Bias currents by +/-10%
  - Time interval as long as 1 week

- ENOB varied less than 0.05-bit

- Gain error not a strong function of bias currents, drift → may not require frequent calibration

- use background calibration to track temperature

Comparison to other 10-b ADCs



- FOM of this work = 0.3pJ/step

Summary

- Low-power gain with capacitive charge-pumps
  - Differential
  - linearity > 10bits
  - Low complexity architecture

Technology	1.8V, 0.18µm CMOS
Input signal swing	1.0V p-p
Area	1.4mm^2
Sampling rate (f_s)	50MS/s
SNDR / SFDR	58.2 dB / 66dB
ENOB	9.4 bits
Power / FOM	9.9 mW / 0.3 pJ/step

Acknowledgements

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