9.2 A 50MS/s 9.9mW Pipelined ADC with 58dB SNDR in 0.18µm CMOS Using Capacitive Charge-Pumps

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In the interest of extending battery life in mobile systems that use pipelined ADCs, several power-efficient pipelined ADCs have recently been proposed. The most promising topologies reported thus far are those that substitute the opamp, which is the largest consumer of power in pipelined ADCs, with alternative and more power-efficient circuits. However, opamp-less pipelined ADCs thus far either: 1) require complex nonlinear calibration [1], 2) are single-ended [2], 3) are pseudo-differential [3], or 4) require a sampling scheme that limits linearity (less than 8b ENOB in [3]). In this paper, a low-power pipelined ADC is presented that has significantly lower power consumption than many previous 10b ADCs in the mid-to-high speed range. The ADC does not require power-hungry opamps, and hence achieves similar power savings as in [1-3]. However, unlike prior opamp-free topologies, the ADC: 1) requires only stage-gain digital calibration, 2) uses fully differential pipelined stages, and 3) uses a sampling scheme that can achieve high linearity (SFDR of 66dB and better than 9b ENOB).

To amplify the residue in each pipeline stage without opamps, a technique inspired by capacitive charge-pumps is used. In capacitive charge-pumps, successively larger voltages are attained by sampling a voltage on many capacitors in one clock phase, and connecting each capacitor in series in the next clock phase, i.e. gain is achieved by addition rather than multiplication. Fig. 9.2.1 illustrates an example of how a gain of ~2× can be achieved using this approach. A unity-gain buffer is included to prevent charge sharing between sampling and load capacitors. Using the approach of Fig. 9.2.1, the classic gain-bandwidth trade-off that binds opamp-based approaches is decoupled; gain is achieved by the capacitor arrangement whereas the bandwidth of the output (V_{out}) is determined by the unity-gain buffer and C_{load}. Thus, a gain of 2× can be achieved without compromising the bandwidth, as would otherwise be required in an opamp-based approach. Since bandwidth is to a first order linearly related to power, a power reduction of at least 50% is achieved over opamp-based topologies.

To adapt the amplification technique of Fig. 9.2.1 for use in pipelined ADCs, three design challenges must be addressed: 1) how to avoid amplifying the input offset of each pipeline stage, noting that a small offset in an early pipeline stage could saturate the buffer output at a supply rail in a later pipeline stage; 2) how to account for parasitic capacitors that reduce gain and linearity; and 3) what topology to use for the buffer.

To avoid amplifying offsets, the sampling network in each pipeline stage is arranged such that the differential input is sampled across the sampling capacitors, as shown in Fig. 9.2.2, which illustrates the 1.5b pipeline stage topology. Switch S0 is included in Fig. 9.2.2 to ensure bottom-plate sampling by switches S1 and S2 (to minimize charge injection hence enable high linearity). Since common-mode rejection is implemented in the sampling network rather than the buffers themselves, fully differential buffers are not required, thus the topology suppresses common-mode noise, yet requires no common-mode feedback.

Parasitic capacitors are minimized by using the smallest switches possible to achieve the desired linearity. Sampling capacitors C_s are implemented with metal capacitors so that the gain is determined primarily by linear components. To account for the gain of each stage being different than the ideal 2×, digital calibration is used to estimate and correct the gain error of each pipeline stage. Thus the approach of this work trades analog complexity with digital complexity, which is a good trade-off since technology scaling favours digital circuits.

Although any sufficiently linear buffer topology can be used, source followers are chosen as they are simple to design and verify, yet can achieve >10b linearity for $0.5V_{pp}$ (single-ended) discrete-time inputs. A deep n-well layer (readily available in many digital processes) is used to eliminate the body effect in M1 in Fig. 9.2.2. NMOS source-followers have the advantage of a large g_m, and have an output close to V_{SS}, which allows the bottom-plate switches S1 and S2 to also be NMOS. Since the gate and source move approximately together in a source-follower, the input capacitance of M1 is given primarily by the gate-drain capacitance, which is typically small. Small gate capacitance on M1 improves the linearity of the gain, and also maximizes the pipeline stage-gain (i.e. provides a larger radix), resulting in fewer total pipeline stages to achieve a desired resolution. Switch S3 is included to power off the buffer during the sampling phase Φ_1, thus enabling further power reduction. A front-end S/H is used in this work and also uses a source-follower-based topology as shown in Fig. 9.2.3.

Since the buffer in each pipeline stage is preceded by amplification of the input, the noise power of the buffer (when referred to the input of the pipeline stage) is reduced by the squared gain of the pipeline stage. Hence the buffer adds only a small noise contribution, enabling the use of small sampling capacitors (thus lower power) to meet the desired thermal noise floor.

Fig. 9.2.4 shows the top-level topology of the 10b 50MS/s pipelined ADC that is implemented in a 1.8V, 0.18µm CMOS process; the core area is 2.0×0.7mm^2. Each pipeline stage has a gain of ~1.75×; thus 12 stages are used to ensure more than 1024 quantization levels. Off-chip foreground calibration is used to correct the gain of each pipeline stage. The total power of the ADC is 9.9mW, including 3.9mW from all active circuitry, and 6mW from all clocking and clock-distribution circuits. Reference voltages are generated off-chip and their power is not included. However it is noted that the total average current drawn by the ADC from the reference voltages is only 0.34mA. Fig. 9.2.5 shows the variation of SNDR/SFDR (after calibration) with input frequency. The ADC achieves a peak SNDR/SFDR of 58.2/66 dB, and a peak ENOB of 9.4b, while maintaining more than 9b ENOB for the full Nyquist input bandwidth. Fig. 9.2.5 also provides an FFT plot for an input frequency of 2.41MHz, where it is seen that even-order distortion terms are suppressed, validating the fully differential functionality of the pipelined stages. Fig. 9.2.6 shows the INL of the ADC before and after calibration. Using a figure-of-merit of Power/($2^{ENOB}\times f_s$), the ADC achieves 0.3pJ/conversion-step. A die micrograph is shown in Fig. 9.2.7.

References:

[1] B. Murmann and B.E. Boser, "A 12 b 75 MS/s Pipelined ADC Using Open-Loop Residue Amplification," *ISSCC Dig. Tech. Papers*, pp. 328-329, Feb. 2003

[2] T. Sepke et al., "Comparator-Based Switched-Capacitor Circuits for Scaled CMOS Technologies," *ISSCC Dig. Tech. Papers*, pp. 812-813, Feb. 2006

[3] J. Hu, N. Dolev, and B. Murmann, "A 9.4-bit, 50-MS/s, 1.44-mW Pipelined ADC Using Dynamic Residue Amplification," *IEEE Symp. VLSI Circuits*, pp. 216-217, June 2008.

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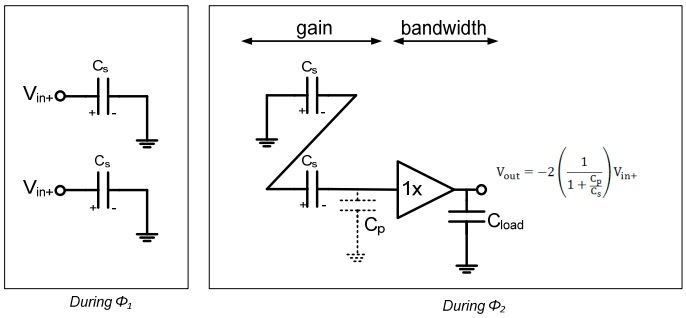

Figure 9.2.1: Gain of near 2× using a capacitive charge-pump approach.

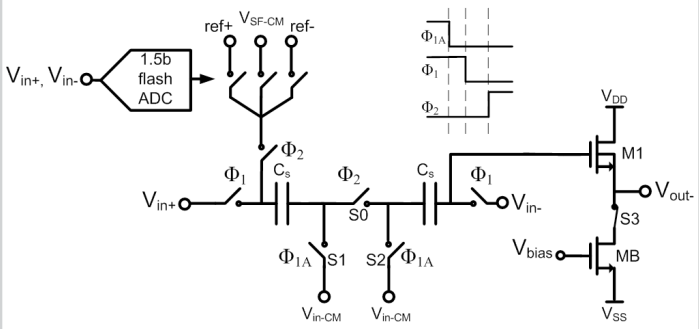

Figure 9.2.2: Topology of each 1.5b pipeline stage. The positive half is shown; the negative half is identical with a reversal of positive/negative signs.

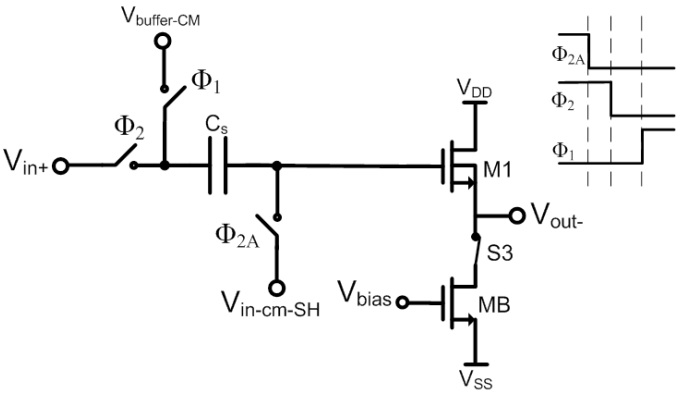

Figure 9.2.3: Source-follower-based sample-and-hold topology.

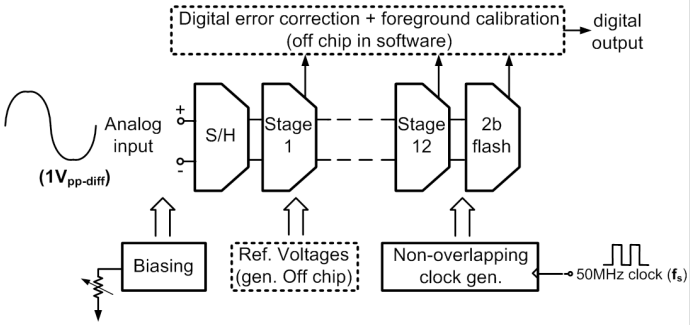

Figure 9.2.4: Topology of the pipelined ADC.

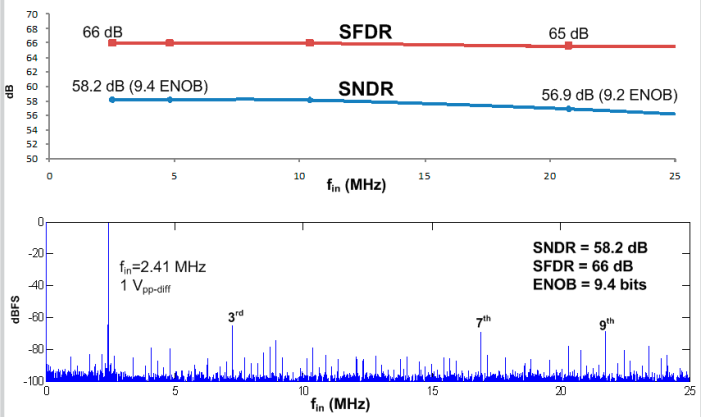

Figure 9.2.5: SNDR and SFDR variation with input frequency, and FFT with f_{in}=2.4MHz (with f_s=50MS/s).

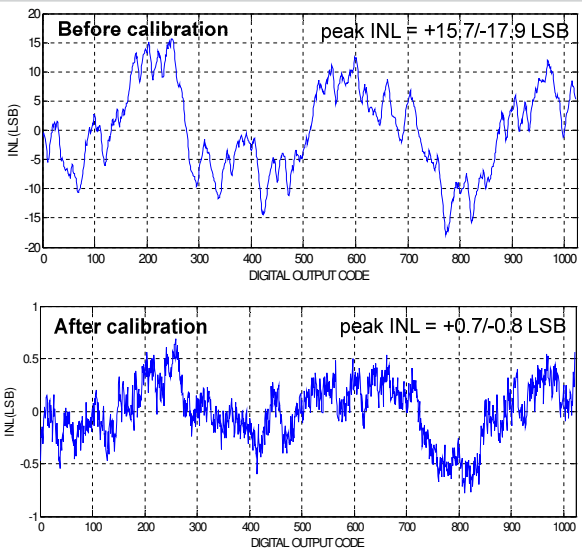

Figure 9.2.6: INL before and after calibration (LSB at the 10b level).

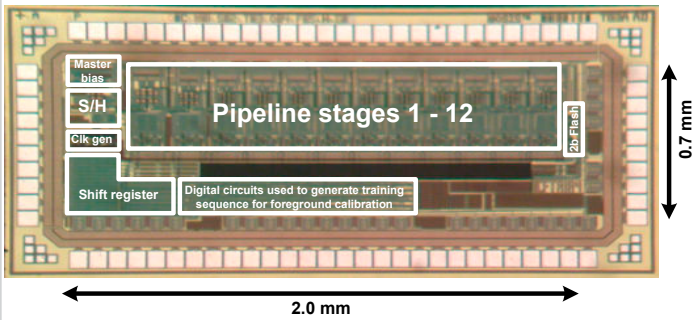

Figure 9.2.7: Die micrograph of ADC.

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