15.3 A 50MS/s (35mW) to 1kS/s (15μW) Power Scaleable 10b Pipelined ADC with Minimal Bias Current Variation

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ADCs that have a power consumption which scales with sampling rate can significantly reduce production costs as a single ADC can be used to target multiple applications with different performance requirements - reducing development costs and time to market. Low-power applications requiring multiple operating speeds and multiple standard compliancy (e.g.: mobile, biomedical) also benefit from a single ADC with scaleable power. ADC power is dominated by analog power, which does not explicitly scale with sampling rate. Previous publications achieve scaleable power in ADCs by making opamp bias currents a function of sampling rate [1], [2]. Although practical for small variations, extending bias current variations to maximize the power scaleable range forces current mirrors into weak inversion, making their drain-source currents much stronger functions of their gate-source voltages [3]. Thus small variations in V_{GS} due to mismatch or noise can significantly alter bias currents, reducing accuracy and yield. Extended bias current variation also increases design/verification time due to multiple design corners. In this paper, a 10b 50MS/s 1.5b/stage pipelined ADC in 0.18μm CMOS is presented that uses a current modulation technique and rapid power-on opamps to enhance the power-scaleable-range of current scaling by 50x, allowing for wide variations in sampling rate with minimal variations in bias current.

If bias currents are unaltered while the ADC sampling rate is decreased, the settling time (t_{settle}) of analog blocks in an ADC becomes a smaller percentage of the period. As a result, the digital outputs of the ADC can be latched after t_{settle}, and the ADC powered down after $t_{settle}+t_{latch}$ (t_{latch} is the time to latch the digital output) as shown in Fig. 15.3.1. Thus the ADC will have an average power of: $P_{avg}= P_{ON} t_{ON} f_s$ ($t_{ON}=t_{settle}+t_{latch}$; P_{ON} is the ADC power consumed during t_{ON}). Lower power for lower sampling rates is achieved by only changing the time the ADC is off ($t_{OFF}=T-t_{ON}$), and without adjusting bias currents, thus strong inversion performance can be retained for low sampling rates. The lowest power achievable with this current modulated power scale (CMPS) approach is limited by blocks that consume non-zero average power during t_{OFF}. The highest sampling rate attainable with CMPS is limited by how quickly the ADC can power on after t_{OFF}.

If bias currents are scaled, CMPS enhances the power-scaleable range of current scaling (Fig. 15.3.1). For example, if current scaling is used to vary ADC power by 1:10, and CMPS allows ADC power to be reduced by 1:50, application of CMPS to the lowest power achievable with current scaling results in a minimum power of $1/(10 \times 50)=1/500^{th}$ the maximum power. The lowest power achievable with CMPS and current scaling is limited practically by how much current scaling can be tolerated.

As the ADC powers off between conversions, after an input is digitized all pipeline stages are reset. Hence when the ADC is powered on again, the next digital output is available after the sampled analog input traverses the entire pipeline (i.e., t_{ON} is the latency of the ADC, t_{lat}). Thus the maximum sampling rate when using CMPS on a pipeline ADC is $1/t_{lat}$. To achieve scaleable power for sampling rates not allowable with CMPS enabled (between $1/t_{lat}$ and $1/t_{stage\text{-}lat}$, where $t_{stage\text{-}lat}$ is the maximum latency of a single pipeline stage), the ADC is operated as a conventional pipeline ADC (i.e., CMPS disabled), where current scaling is used to achieve scaleable power for the narrow range of non-CMPS sampling rates.

A block diagram of the overall power scaleable ADC is shown in Fig. 15.3.2. When CMPS is enabled, only one pipeline stage is powered on at a time as shown in Fig. 15.3.3, as only one analog sample is digitized every T_s (i.e. the ADC operates similar to an algorithmic ADC). A digital state machine is used to sequence the active times of each pipeline stage where T_s is digitally programmable. The settling time for each stage (t_{stage}) is equal to the pulse width of the clock supplied to the state machine (f_{sm}). As the state machine consumes power during t_{OFF}, it limits the lowest power achievable with CMPS, however the power can be reduced by reducing f_{sm}.

The key challenge for CMPS to be feasible at high speeds is to be able to rapidly power on and off the sample-and-hold/Multiplying DAC opamps, and their bias circuits (reference voltages are generated off chip and are not addressed in this work). Using a replica bias technique, a rapid-power-on opamp is proposed and shown in Fig. 15.3.4. Switching a copy of the bias voltage to an opamp current source, rather than the bias voltage itself, results in short power-on times because the master bias voltage is is isolated from switching-induced perturbations and the replica bias isolated from the large capacitance of the original bias voltage. Since replica biasing can be arranged to increase current source resistance, a large DC gain is achieved using a single-stage folded-cascode gain-boosting architecture, affording simple load compensation and passive common-mode feedback. Series current switching is used to modulate replica biasing opamp power and tail current transistors without affecting the signal swing at the output of the opamp. Additional switch transistors in Fig. 15.3.4 are used to decrease off time, and avoid floating nodes when the opamp powers off.

Due to longer power-up times, biasing circuits are powered on before the sample-and-hold ($t_{bias\text{-}lead}$ in Fig. 15.3.3), resulting in a conversion latency of 9 clock cycles. Thus the minimum amount of current scaling required for continuous power scaleability is for f_s between 50MS/s and 50/9=5.55MS/s. Bias circuit power is modulated by series current switches.

The ADC was fabricated in a 0.18μm 1.8V CMOS process, occupying $1.2mm^2$ of active area. To demonstrate the multiplying nature of CMPS, bias currents are scaled up to 1:50 and CMPS is applied with f_{sm}=50MHz, 5.55MHz, and 1MHz. The measured power and SNDR versus sampling rate are shown in Fig. 15.3.5. Figure 15.3.5 shows that CMPS enhances the power-scaleable range of current scaling by 50×, where the lowest power for a given f_{sm} is limited by the power of the digital state machine. The ratio of maximum (35mW, 50MS/s) to minimum power (15μW, 1kS/s) achievable when using CMPS with current scaling is ~1:2500. From Fig. 15.3.5, for a given f_{sm} and bias current, SNDR is virtually constant due to the constant settling times between different sampling rates. Figure 15.3.6 shows the performance at the maximum speed of 50MS/s, where an SNDR of 55dB is achieved at f_{in}=20.94MHz, and SFDR of 67dB. The INL at f_s=50MS/s was +1.06/–1.2LSB, and DNL +0.63/–0.91LSB.

References:

[1] K. Gulati, H.S. Lee, "A Low-Power Reconfigurable Analog-to-Digital Converter," *IEEE J. Solid-State Circuits*, vol 36, pp. 1900-1911, Dec., 2001.
[2] B. Hernes et al., "A 1.2V 220MS/s 10b Pipeline ADC Implemented in 0.13μm Digital CMOS," *ISSCC Dig. Tech. Papers*, pp. 256-257, Feb., 2004.
[3] C. C.Enz and E. A.Vittoz, "CMOS Low-Power Analog Circuit Design," *Proc. 1996 IEEE Int. Symp. Circuits and Systems (ISCAS'96)*, ch. 1.2, Tutorials, pp. 79-133.

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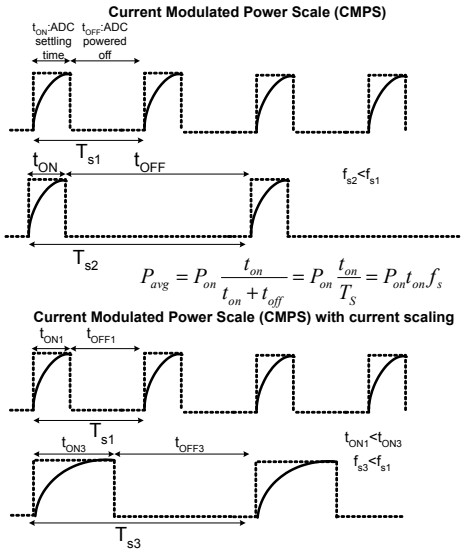

Figure 15.3.1: Current modulated power scale (CMPS).

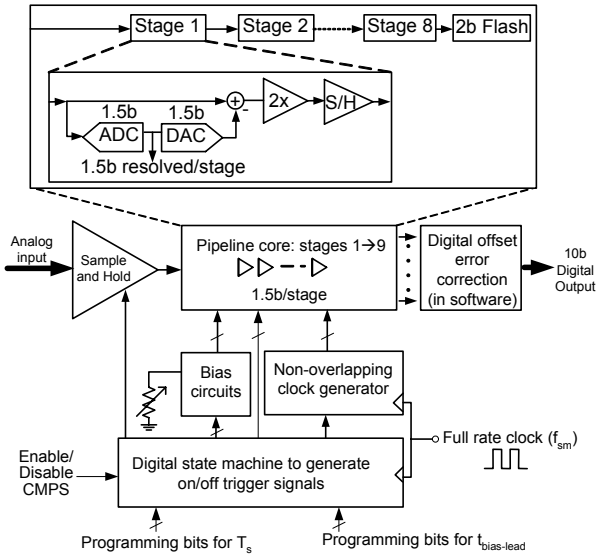

Figure 15.3.2: System level diagram of power scaleable ADC.

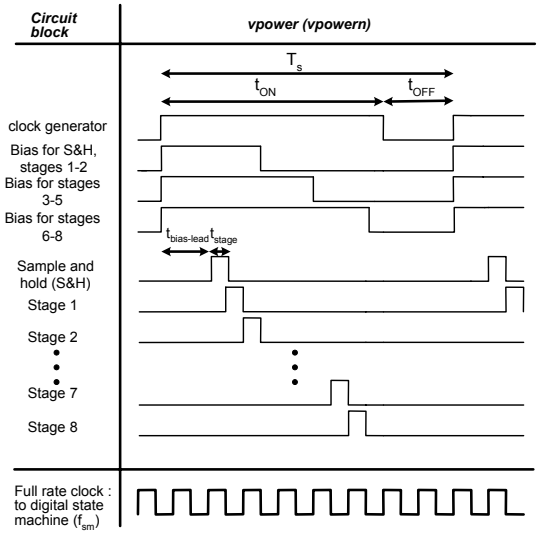

Figure 15.3.3: Power on/off timing diagram of blocks in ADC.

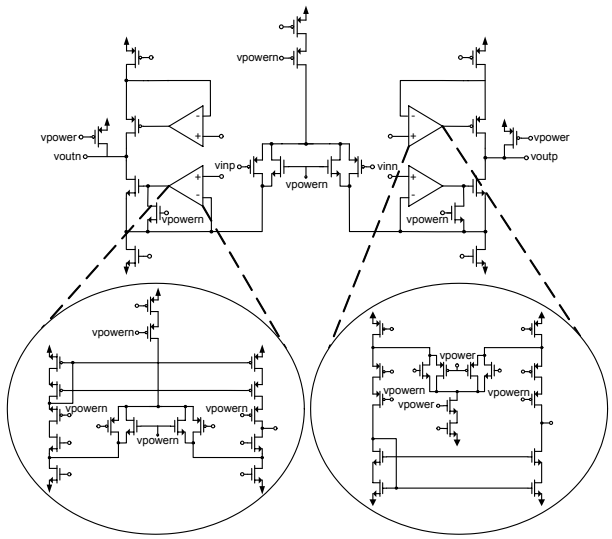

Figure 15.3.4: Rapid power on/off opamp schematic.

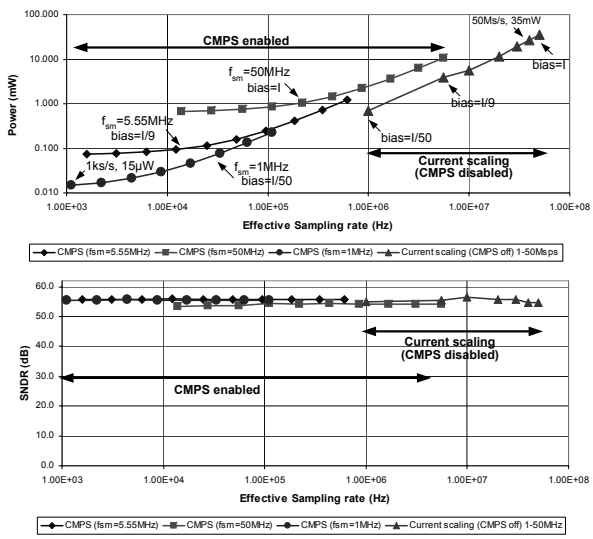

Figure 15.3.5: Power & SNDR versus sampling rate for f_{sm}=1, 5.55, 50MHz.

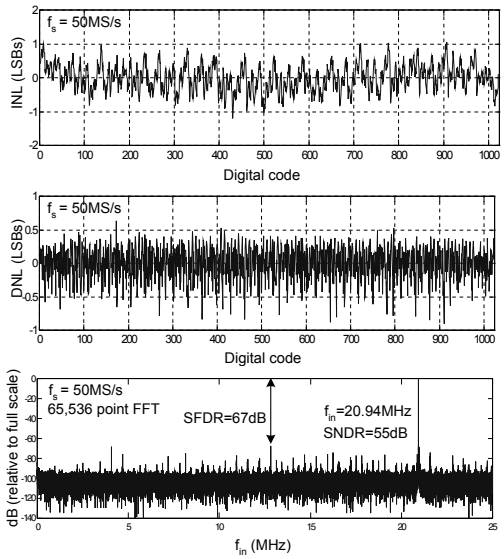

Figure 15.3.6: INL, DNL, FFT of digital output for f_s=50MS/s.

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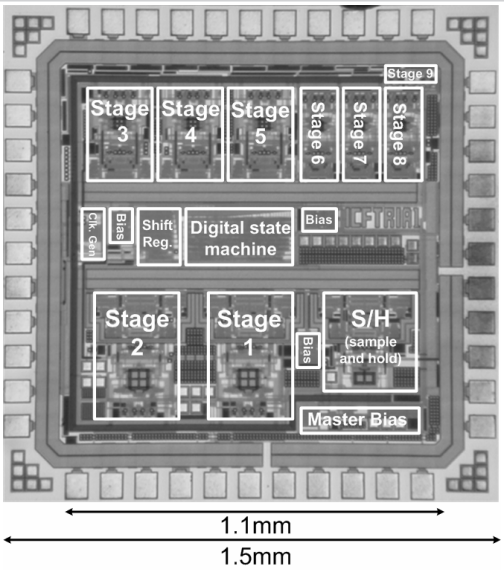

Fig. 15.3.7: Power scaleable ADC chip micrograph.

